Title: Voltage Controlled Quadrature Oscillator with Phase Tuning

Description of the Figures

Figure 1 is a block diagram of a differential 2 stage ring oscillator with variable quadrature output phases according to the present invention.

Figure 2 is a schematic of the circuit of Figure 1.

Figure 3 is a schematic of a differential regenerative frequency divider according to the present invention.

Figure 4 is a block diagram of an image reject mixer.

Figure 5 is a block diagram of an improved image reject mixer according to the present invention.

Detailed Description of the Preferred Embodiments

Figure 1 shows a differential 2 stage ring oscillator 20 with quadrature output phases. Oscillator 20 includes a ring oscillator 21 and two current sources 28, 30. Ring oscillator 21 includes a pair of differential amplifiers 22 and 24 which are connected together as a ring oscillator. The propagation delay τ_A of amplifier 22 is controlled by varying the current of controllable current source 28 and the propagation delay τ_B of amplifier 24 is controlled by varying the current of controllable current source 30. The oscillation frequency of ring oscillator 21 is inversely related to the total propagation delay ($\tau_A + \tau_B$) of amplifiers 22 and 24. Signal V_1 is measured across nodes V_{1+} and V_{1-}. Signal V_2 is measured across nodes V_{2+} and V_{2-}. If the propagation delays, τ_A and τ_B, of amplifiers 22 and 24 are equal, then signal V_2 will lag 90° behind signal V_1 (i.e. signals V_1 and V_2 will be quadrature signals). Propagation delay τ_A of amplifier 22 can be changed by adjusting the current of current source 28. Similarly, propagation delay τ_B of amplifier 24 can be changed by adjusting the current of current source 30.

The frequency of ring oscillator 21 may be varied, without affecting the phase difference between signals V_1 and V_2, by adjusting the currents of current sources 28 and 30 proportionally.

The phase difference between signals V_1 and V_2 may be varied by differentially adjusting the propagation delays, τ_A and τ_B, of amplifiers 22 and 24. This is done by differentially adjusting the currents of current sources 28 and 30.

Figure 2 is a schematic diagram of circuit 10. Amplifier 22 comprises a pair of emitter coupled amplifiers Q_1 and Q_2. Amplifier 24 comprises a pair of emitter coupled transistors Q_3 and Q_4. The collectors and bases of transistors $Q_1 - Q_4$ are connected to form differential ring 21. The collectors of Q_1 and Q_2 are coupled to a voltage source V_{cc1} through resistors R_1 and R_2. The collectors of Q_3 and Q_4 are coupled to voltage source V_{cc2} through resistors R_3 and R_4.

Current source 28 comprises a transistor Q_5. The base of transistor Q_5 is coupled to at input voltage V_{bias1}, which controls the current of current source 28. Similarly, current source 30 comprises a transistor Q_6. The current of current source 30 is controlled by voltage signal V_{bias2}. Voltage signals V_{bias1} and V_{bias2} must have a

As the level of voltage signal V_{bias1} is increased, the current of current source 28 will increase. This will increase the switching speed and decrease the propagation delay of differential amplifier 22. Similarly, the switching speed and propagation delay of differential amplifier 24 are controlled by varying the level of voltage signal V_{bias2}.

Although the propagation delays of amplifiers 22 and 24 are described here as being controlled by varying the bias currents of the amplifiers (i.e. the currents of current sources 28 and 30), the same results may be attained by creating any imbalance in the electrical symmetry between amplifiers 22 and 24. For example: a bias voltage or current may be altered at any node of ring oscillator 21. Alternatively, a controllable capacitor, inductor or resistor may be coupled to any node to differentially alter the internal impedances in amplifiers 22 and 24.

Ring oscillator 21 may also be implemented as a pair of quadrature coupled differential oscillators.

Figure 3 shows a differential regenerative (i.e. dynamic) divider 50 with quadrature output. This circuit is identical to circuit 20, except that the bases of transistors Q_5 and Q_6 are additionally coupled to an input signal V_{in} at nodes 52 and 54 through coupling capacitors C_{c1} and C_{c2}.

Signal V_{in} is received at nodes 52, 54 and has a frequency f_{in}. Transistors Q_5 and Q_6 convert input signal V_{in} into an alternating current signal i_{in} which is injected into emitter coupled nodes 56 and 58 of amplifiers 22 and 24. The frequency of current signal i_{in} is the same as the frequency f_{in} of input signal V_{in}. This injection locks ring oscillator 21 such that the oscillation frequency f_{osc} of the ring oscillator is half the input frequency f_{in} of input signal V_{in}.

If the propogation delays τ_A and τ_B of amplifiers 22 and 24 are configured to be the same, then signals V_1 and V_2 will be quadrature phased signals (i.e. they will be separated in phase by 90°).

The phase relationship between V_1 and V_2 can be altered, without altering the frequency of ring oscillator 21 by differentially altering input voltages V_{bias1} and V_{bias2}. Since ring oscillator 21 is injection locked to frequency $f_{in}/2$, it is only necessary to vary one of the input voltages V_{bias1} or V_{bias2}, with respect to the other, to vary the phase relationship between V_1 and V_2.

In radio system architectures, image reject mixing requires accurate quadrature local oscillator signal generators to attain high image rejection performance. This is required for both up (transmitter) and down (receiver) conversions. Known designs attempt to design the quadrature signal generator (frequency divider) to produce as accurately as possible a pair of signals (generally referred to as the inphase (I) and quadrature (Q) signals) which are separated by precisely 90°. It is impossible to account for all process tolerances which can impair the image rejection performance of an image reject architecture. Approximately 1° of phase error is common. This translates to a maximum image rejection of about 46 dB. Including other sources of phase and amplitude error in the quadrature down conversion path a typical specification for image rejection is approximately 35 dB. In order to improve image rejection beyond this level, a system is required for controlling the phase relation between the I

and Q local oscillator signals with a high degree of precision. This system may be used to provide $\bar{I}$ and $\bar{Q}$ signals which have a phase relation which compensates for the other sources of phase error. In a particular case, the phase relation between the I and Q signals may be greater or less than 90°.

Figure 4 is a block diagram of an image reject mixer 100 using the Hartley topology. Signal RF_{in} comprises a RF signal having a frequency f_{RF} and an image signal having a frequency f_{IM}. Signal generator 101 provides a pair of local oscillator signals V_1 (which takes the place of the I signal) and V_2 (which takes the place of the Q signal), both having the same frequency f_{LO}. Signals V_1 and V_2 have phase angles ϕ_{V1} and ϕ_{V2}. ϕ_{V1} is arbitrarily chosen as a reference for 0° phase. Signals V_1 and V_2 are mixed with the received signal RF_{in} in mixers 102 and 104 to provide a pair of signals IF_1 and IF_2. When high side injection is used (f_{LO} is greater than f_{RF}), the IF_1 signal comprises the RF signal converted to frequency ($f_{LO} - f_{RF}$) and the image signal (sideband) converted to frequency ($f_{IM} - f_{LO}$). Signal IF_2 comprises the RF signal converted to frequency ($f_{LO} - f_{RF}$) and shifted in phase by $\phi_{V2}°$ and the image signal converted to frequency ($f_{IM} - f_{LO}$) and shifted in phase by $-\phi_{V2}°$.

The amplified signals IF_1 and IF_2 are combined by a quadrature combiner 110. Quadrature combiner 110 is designed to complete the image rejection by providing a phase shift ϕ_{QC1} to signal IF_1 and a phase shift ϕ_{QC2} to signal IF_2. Ideally, to maximize suppression of the image signal, $\phi_{QC1} - \phi_{V1} = 0°$ and $\phi_{QC2} + \phi_{V2} = -180°$ (assuming high side injection). Ideally, $\phi_{V2} - \phi_{V1} = 90°$, $\phi_{QC2} - \phi_{QC1} = 90°$. In known quadrature combiners, $\phi_{QC2} - \phi_{QC1}$ is generally not 90°. Typically a phase error exists, and the image is not maximally suppressed. In addition, known quadrature combiners also introduce amplitude errors in the IF_1 and/or IF_2 signal paths. For example, both signal IF_1 may be reduced in amplitude by N dB.

Current state of the art systems attempt to maintain the 90° phase separations between ϕ_{V1} and ϕ_{v2} and between ϕ_{QC1} and ϕ_{QC2}. It has been found that image rejection performance can be substantially increased by adjusting the phase difference to compensate for the phase error in the quadrature combiner

110. In addition, amplitude errors in the IF_1 and IF_2 signal paths can be compensated for.

Figure 5 shows an improved image reject mixer 200. Components of image reject mixer 200 which correspond to components of image reject 100 are identified by the same reference numerals. Signal generator 101 of image reject mixer has been replaced with circuit 50 (Figure 3). Nodes 52 and 54 of circuit 50 are coupled to a signal generator 202.

Output signal IF_{out} is received by a carrier level detector 203. Carrier level detector provides a signal to feedback controller 204. Feedback controller provides control signals to switches SW_1 and SW_2, calibration signal transmitter 206, signal generator 202, amplifiers 210, 212 and provides voltage signal V_{bias1} and V_{bias2}. Image reject mixer has a calibration mode and operation mode.

Initially, in the calibration mode the following configuration is set by controller 204:

(a) switches SW_1 and SW_2 are configured to connect calibration signal transmitter 206 to input node RF_{in};

(b) signal generator 202 is configured to produce a signal with a frequency twice that required for the local oscillator signals V_1 and V_2; and

(c) voltage signals V_{bias1} and V_{bias2} are configured to initiate the operation of circuit 50 with the phase delays of amplifiers 22 and 24 being approximately equal; and

(d) calibration signal transmitter 206 is configured to generate a signal at the frequency of the image;

(e) the gains of amplifiers 210 and 212 are set equal.

Controller 204 then runs a calibration algorithm. Signal IF_{out} is generated as in image reject mixer 100. Signal IF_{out} will contain the image signal generated by calibration signal generator 206. The level of signal IF_{out} will correspond to phase and amplitude errors introduced in quadrature combiner 110 and other components of image reject mixer 200. Carrier level detector provides a signal corresponding to the level of signal IF_{out} to controller 204.

Controller 204 then adjusts the relative propagation delays of amplifier 22 and 24 (within circuit 50) to control the relative phase difference between V1 and V2 to reduce the signal level of IF_{out} as much as possible. Controller 204 than adjusts the relative gains of amplifiers 210 and 212 to reduce the signal level of IF_{out} as much as possible. Controller 204 then alternately attempts to reduce the signal level of IF_{out} by adjusting the phase difference between V_1 and V_2 and by adjusting the relative gains of amplifiers 210 and 212. When no further reduction of IF_{out} is attained for several iterations, the calibration mode is terminated by configuring switches SW_1 and SW_2 to disconnect the calibration signal transmitter 206 from node RF_{in} and to connect the antenna to node RF_{in}.

Image reject mixer 200 then enters the operation mode. The setting for the phase difference between V_1 and V_2 and the relative gains of amplifiers 210 and 212 determined during the calibration mode are retained during the operation mode to maintain the improved image reject performance of image reject mixer 200 attained during calibration mode.

Image reject mixer 200 may be integrated. The functionality of the elements of image reject mixer 200 contained within dashed boundary 216 may wholly or partially implemented using analog or digital technology.

In addition, image reject mixer 200 may be used with a transmitter.

WA 19.3 A 2V 5.1-5.8GHz Image-Reject Receiver with Wide Dynamic Range

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Worldwide spectral allocations in the 5-6GHz band for short range, high-speed digital communications are broadening the scope of wireless applications. RF IC technology is needed to meet the aggressive cost, size and power consumption targets demanded by applications such as portable Internet access.

A 5-6GHz image-reject receiver IC implemented in 0.5μm 25GHz silicon bipolar technology draws 20mA from a 2V supply. The image rejection obtainable with this IC is sufficient to eliminate the off-chip interstage RF filter in a heterodyne receiver, thereby simplifying packaging requirements and decreasing costs. The methods used here that make this design possible are: regenerative frequency doubling, I-Q phase error compensation and RF interstage coupling. Low-voltage circuit topologies are used throughout to minimize power consumption and ensure compatibility with deep sub-micron CMOS (baseband) ASICs operating from low-voltage supplies.

Components implemented on-chip are enclosed by the dashed boundary shown in Figure 19.3.1 (note that only active devices for a VCO are integrated). Two stages of regenerative frequency doubling followed by a frequency halver (i.e., analog divide-by-two) generate LO signals in precise phase quadrature (I and Q). Two-stage multiplication allows a lower fundamental LO to be used (2.6-3.4GHz) for better phase noise performance. These signals drive dual mixers to downconvert the received signal. Image rejection is obtained by quadrature addition of the downconverted signals directly at baseband in a homodyne receiver, or through quadrature combining at an IF.

The regenerative method of frequency doubling is illustrated in Figure 19.3.2. A 2-stage quadrature ring oscillator has its fundamental oscillation mode injection-locked to the input signal, f_{in}. The outputs of each stage are then squared by individual multipliers resulting in a differential output at $2f_{in}$. This circuit is implemented with two differential amplifiers connected in a positive feedback loop as shown in Figure 19.3.3. The large-signal non-linearity of each differential pair gives a strong common-mode ($2f_{in}$) signal at the emitter outputs. In the receiver IC, cascaded doubler stages multiply the VCO signal by a factor of 4, with a maximum operating frequency that is greater than $f_t/2$ (up to 13.6 GHz).

Figure 19.3.4 shows the regenerative divide-by-2 circuit [1]. A 2f input signal is injected into the emitters of each differential amplifier by Q11 and Q12. This causes the quadrature oscillator formed by transistor pairs Q7-Q10 to cycle at one-half the frequency of the injected currents (reverse action to the doubler). Unlike the asymmetric injection of the doubler, symmetry in the halver results in a pair of quadrature-phased LO signals at nodes $I/\overline{I}$ and $Q/\overline{Q}$ with minimal phase error.

Image rejection in the receiver is improved by trimming the amplitude and phase relationship between I and Q signals at IF. This is realized by adjusting the phase angle between LO signals using the ratio of bias currents flowing in Q11 and Q12. Unlike R-C phase control methods, this technique of phase tuning is relatively independent of the operating frequency. Amplitude errors at the receiver output are also compensated by varying the gain in either the RF, LO or IF signal paths thereby allowing over 80dB of rejection to be realized.

Figure 19.3.5 shows a complete schematic of the signal path including off-chip IF matching and quadrature combining circuits used to evaluate the IC. Parasitics for the 32-pin CQFP package are not shown but are accounted for in the design. The RF LNA/mixers[2] are coupled by a monolithic transformer (T1) with a non-integer turns ratio that substantially increases the overall gain available from the receiver. This symmetric tri-filar design consists of 8 turns of top-metal and measures 300μm per side.

LNA transistors Q1 and Q2 are driven differentially to reduce the effects of wirebond and package inductances at 5-6GHz. Moreover, the Q-factor of emitter inductor, Lee increases by about 50% when excited differentially[3]. The LNA design employs both series and shunt feedback so that a coincident noise and power match is realized. Each BJT is biased at 2.5mA and has a $20x0.5\mu m^2$ emitter area. The doubly-balanced mixers (Q3-Q10) are also biased at 2.5mA each, giving a load impedance of 300-400Ω/side for the LNA when reflected through T1. A noise figure of 2.2dB and 14dB power gain is achieved for the LNA. The measured SSB (50Ω) noise figure of the receiver is 5.1dB with 15dB conversion gain and IIP3 of -9.5dBm at 5.3GHz. There is only a slight degradation in performance at 5.8GHz. Input return loss is better than 14dB across the band.

The 75MHz IF used for testing is based on component availability. Discrete component tolerances limit the wideband image rejection to more than 45dB over a 5MHz bandwidth, with 80dB rejection at the band center (a relative IF bandwidth of 6.7%). 80dB image rejection implies that the I-Q phase error is less than 0.011°. To determine the variation of LO phase angle as a function of frequency, the RF and LO are swept while keeping the IF constant (to eliminate the IF errors). Greater than 60dB rejection (or <0.11° total phase error) over a 400MHz RF-LO sweep is achieved without re-adjusting the amplitude or phase balance after initial trimming.

Figure 19.3.6 compares the measured performance of this receiver to other image-reject receivers designed for operation in the 5-6GHz band. All measurements are for the packaged device in a 50Ω test fixture. Figure 19.3.7 displays the chip micrograph.

Acknowledgments:
This work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC) and Micronet. IC fabrication by Nortel Semiconductor was facilitated by the Canadian Microelectronics Corporation.

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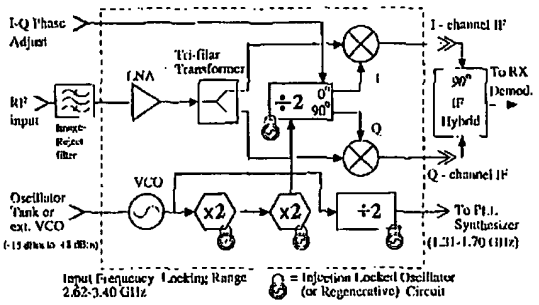

Figure 19.3.1: Image-reject receiver block diagram.

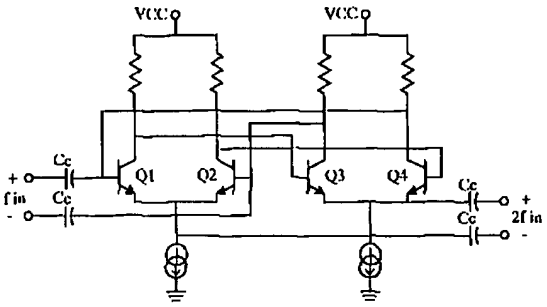

Figure 19.3.2: Regenerative frequency doubler.

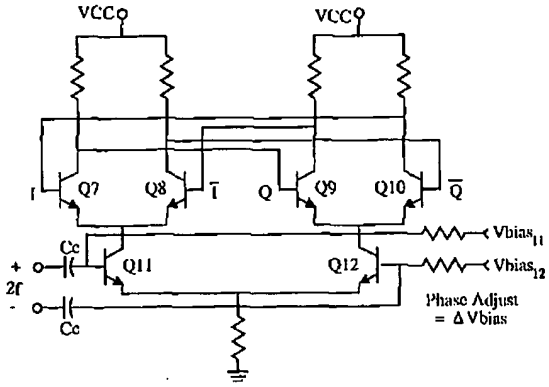

Figure 19.3.4: Regenerative frequency halver.

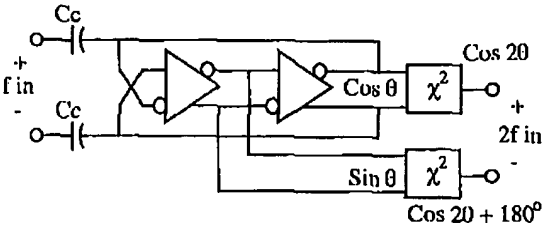

Figure 19.3.3: Injection locked ring oscillator.

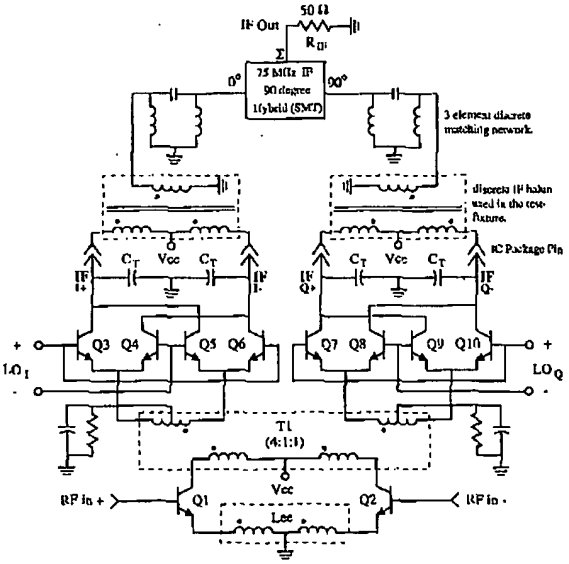

Figure 19.3.5: RF front-end and IF test circuit.

Figure 19.3.7: See page 468.

Parameter	Measured	Measured	Ref. [4]	Ref. [5]
Technology f_T, GHz	25		22 GHz BiCMOS	45
RF Input, GHz	5.3	5.8	5.1-5.4	5.15 - 5.35
VCO Frequency, GHz	2.6875	2.9375	2.15 - 2.35	4.85 - 5.05
IF, MHz	75		400	300
Conversion Gain, dB	15.1	14.9	18	11.7
RF Input Return Loss, dB	14	14.6	-	8.6
SSB Noise Figure (50Ω), dB	5.1		7 dB (SSB?)	7.5 (DSB)
Input IP3, dBm	-9.4	-10.5	-16	-18.5
Fundamental LO to RF Isolation, dB	60	60.5	-	53.5
Doubled LO to RF Isolation, dB	75	74	-	no doubler
RF to IF Isolation, dB	67	68	-	63.5
Supply Voltage, V	2.2		3	3.3
Power Dissipation, mW	44.4		55.5	122
Chip Area, mm²	1.9 x 1.2		3.0 x 2.4 (TX and RX)	2.07 x 2.77
Image Rejection, dB	80 (maximum rejection at center of IF)		off-chip filtering required	21.3 (setup limited)

Figure 19.3.6: Measured receiver performance and comparisons.

A Low-Voltage 5.1–5.8-GHz Image-Reject Receiver with Wide Dynamic Range

James P. Maligeorgos and John R. Long, *Member, IEEE*

***Abstract*—A monolithic 5–6-GHz band receiver, consisting of a differential preamplifier, dual doubly balanced mixers, cascaded injection-locked frequency doublers, and a quadrature local oscillator generator and prescaler, realizes over 45 dB of image-rejection in a mature 25-GHz silicon bipolar technology. The measured single sideband (50 Ω) noise figure is 5.1 dB with an IIP3 of −4.5 dBm and 17-dB conversion gain at 5.3 GHz. The 1.9×1.2 mm^2 IC is packaged in a standard 32-pin ceramic quad flatpack and consumes less than 50 mW from a 2.2-V supply.**

***Index Terms*—Image-reject mixing, low-noise amplifiers, low-power design, low voltage design, RFIC design, simultaneous noise/power matching, wireless receivers.**

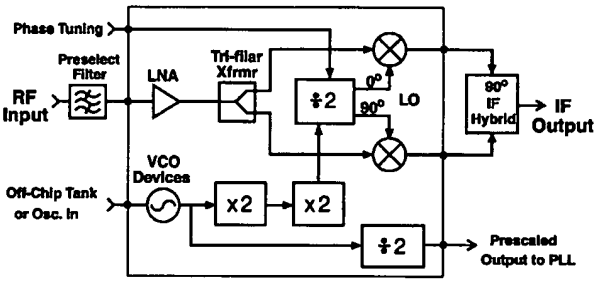

Fig. 1. Receiver front-end block diagram.

I. Introduction

THE SUCCESS of cellular telephony and the Internet has resulted in greater demand for high-speed wireless connectivity. Spectral allocations in the 5–6-GHz band offer 300–400 MHz of unlicensed spectrum in many regions [1], [2], with the potential to realize both fixed and portable wireless multimedia applications at data rates between 20–150 Mb/s. Radio frequency integrated circuit (RF IC) technology is needed to meet the aggressive cost, size, and power consumption targets demanded by these applications.

This paper describes a single-chip 5.1–5.8-GHz image-reject receiver fabricated in a mature medium-performance (25-GHz f_T) 0.5-μm silicon bipolar technology. Designed for operation from a single sub-3-V supply, the receiver IC incorporates a fully differential low-noise preamplifier (LNA), dual doubly balanced mixers, a local oscillator (LO) divide-by-two prescaler, and the active elements needed to implement a voltage-controlled oscillator (VCO). An on-chip three-filament (trifilar) transformer couples the LNA and mixers, allowing improved gain and linearity and lower overall noise figure and power consumption compared to conventional IC designs. A new technique for low-power regenerative frequency doubling multiplies the LO reference source by a factor of either two or four. A companion analog divide-by-two or frequency divider circuit is designed for low-voltage operation and generates in-phase (I) and quadrature (Q) LO signals in the 5–6-GHz band. An important feature of the divider circuit is its ability to realize precise adjustments of the phase relationship between I and Q LO components. A regenerative divide-by-two prescaler (with output buffer) enables an $f_{LO}/4$ output to drive external PLL synthesizer ICs designed for operation below 2 GHz (i.e., commercially available PLL synthesizer ICs).

II. 5–6-GHz Receiver Architecture

The frequency allocations for unlicensed operation in North America (UN-II) have been split into two bands: 5.15–5.35 and 5.725–5.825 GHz [1], [3]. However, in Europe the HiperLAN standard specifies the upper band at 5.47–5.725 GHz [2]. Other potential applications lie in the 5.8–5.9-GHz region, where international allocations have been made for intelligent transportation system (ITS) services using dedicated short-range communications [3]. The objective for this work is a monolithic implementation that covers the entire 5–6-GHz band in order to widen the scope of applications for the IC.

Fig. 1 shows a block diagram of the receiver RF IC. The functions indicated within the bounded region have been implemented on-chip. Balanced circuitry is used throughout the IC to reduce crosstalk between the circuit blocks. This doubles the power consumption for many of the circuit functions (e.g., LNA) compared to conventional single-ended realizations, and therefore low-voltage circuit topologies are emphasized to conserve power in portable equipment. Low-voltage operation is also desirable to maintain compatibility with receiver backend signal processing circuits that will likely be implemented in deep-submicron CMOS technologies. In the 5–6-GHz band, the gain available in the RF front-end is restricted by limitations of the 25-GHz technology used for this implementation [4]. The on-chip interstage coupling transformer improves the efficiency of the RF circuits (i.e., dynamic range for a given supply voltage/bias current in the LNA and mixer) through resonant

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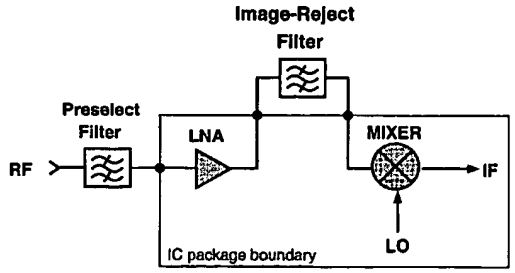


Fig. 2. Conventional heterodyne receiver IC front-end.

parasitic absorption, and allows operation at supply voltages as low as 0.9 V. This topology has been described previously in [5] and [6]. A standard 32-pin quad flatpack (QFP) was selected to package the IC to reduce costs at the expense of larger parasitics at 5–6 GHz (e.g., lead and bondwire inductances).

Quadrature (0° and 90° phased) LO signals are required to drive the doubly balanced mixers. The divide-by-two circuit in Fig. 1 generates these two LO phases. The double-frequency drive signal for the divider is derived from cascaded frequency doublers. The fundamental LO is multiplied by 4 and then divided by 2, for a net $\times 2$ multiply (e.g., a 2.75-GHz LO is scaled to 5.5-GHz I and Q signals at the mixer LO inputs). A cascade of multipliers allows the option of using a single multiply-by-two followed by the divider to service the 2.4-GHz ISM band. Thus, this LO scheme could service both 2.4 and 5–6-GHz bands. However, this option was not pursued for this work. Note that only the active devices for the VCO are implemented on-chip.

A. RF Filtering and Image Rejection

Downconversion in a heterodyne receiver translates signals from both the "image" and RF bands to the same intermediate frequency (IF), as both bands share the same frequency difference with respect to the LO. To eliminate the possibility of interference from the image band, image-reject (IR) filters tuned to the RF band are inserted in the signal path ahead of the mixer, as shown in Fig. 2. However, in a highly integrated receiver module the interstage IR filter introduces losses in the RF signal path, adding cost, packaging complexity, and power consumption through the additional 50-Ω interface. Off-chip fixed-frequency filters also limit system flexibility in an open standard environment. In addition, a 5–6-GHz band receiver operating at MB/s data rates will likely require a much wider IF bandwidth than today's 2.4-GHz ISM band systems.

Monolithic techniques, such as VCO tracking notch filters [7], [8], image-reject or single-sideband mixing [9], and direct-conversion [10] receivers do not require the interstage IR filter. However, the complexity in implementation must be weighed against other constraints such as cost and performance. For example, a fully differential receiver employing tracking notch filters was recently reported by Copeland [8]. This design uses 14 monolithic inductors (excluding VCO) and therefore requires a relatively large chip area (approximately 4 mm^2). In addition, a high IF on the order of 1 GHz is used to separate the RF and image bands to prevent the notch filter from attenuating the desired RF signal.

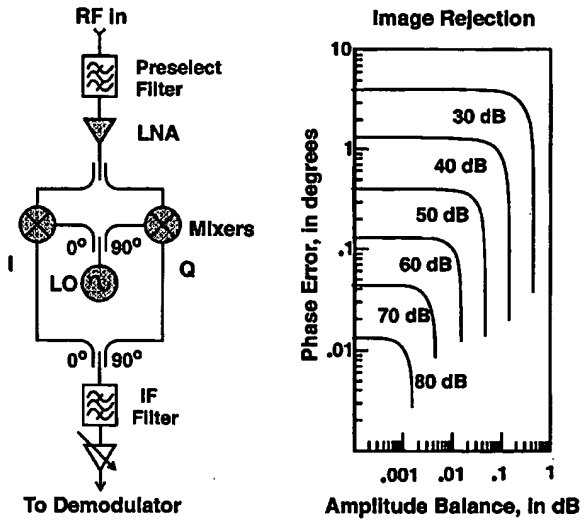


Fig. 3. Image-reject (Hartley) receiver front-end. (a) Hartley receiver downconverter. (b) Image rejection versus amplitude and phase errors in quadrature signals.

An alternative to electronic filtering is image-reject downconversion (see Fig. 3), which is the method chosen for this work. A preselect filter bandlimits the spectral input to the LNA to help prevent overloading or desensitization and suppresses out-of-band interferers. It also provides some rejection of the image if the receiver is designed to have a first IF greater than the width of the preselect filter's passband. The filtered RF signal is then amplified by the LNA, and coupled to two downconverting mixers. Quadrature LO signals drive each mixer, producing in-phase and quadrature IF outputs. The image band is rejected if the I and Q mixer outputs are then summed in phase quadrature; the resulting image suppression as a function of phase and amplitude errors between the I and Q LOs is illustrated in Fig. 3(b). Note that the interstage off-chip filter is no longer required if the combined rejection from the preselect filter and IR mixing stages is sufficiently high. Of course, the I and Q mixer outputs could also be used at baseband (as in a direct conversion receiver) by appropriate selection of the LO frequency. Thus, a distinct advantage of this approach is its ability to address both direct conversion and heterodyne architectures.

B. Quadrature Signal Generation

Quadrature LO signals are often generated using a digital divide-by-two flip-flop [9] or an *RC* polyphase network [11] in systems where the quadrature LO cannot be directly obtained from the VCO. For 40 dB of image rejection, the phase and amplitude errors must be controlled to within 1° and 0.1 dB, respectively, over the entire range of input frequencies [see Fig. 3(b)]. A regenerative frequency divider (analog divide-by-two) with quadrature outputs [12] was selected for this design. Compared to an *RC* polyphase filter (for quadrature signal generation), the regenerative technique is less susceptible to process gradients and tolerances, requires less chip area, provides signal gain, and affords precision phase tuning control over about one octave in frequency. The analog method of division is preferred over the

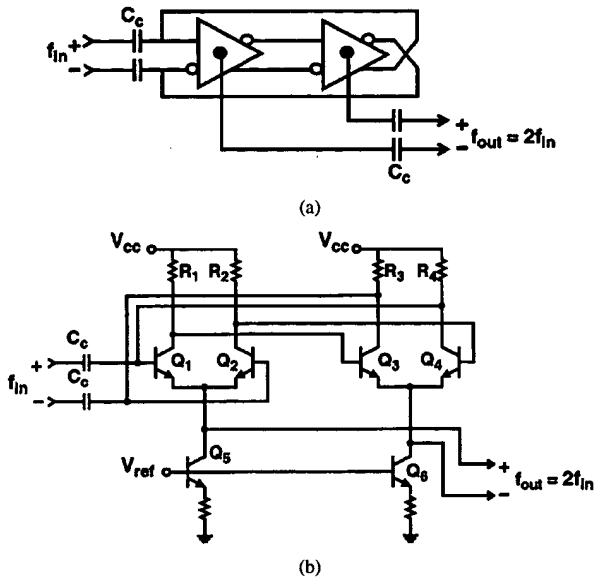


Fig. 4. Regenerative frequency doubler. (a) Block diagram. (b) Simplified schematic diagram.

more common digital master–slave frequency dividers because of lower power consumption and degradation in phase noise, quieter operation (less spurious content and crosstalk with other circuit blocks), and higher maximum operating frequency [13]. However, using a divide-by-two method to generate I and Q signals requires an input signal that is at least twice the frequency of the desired output. For a 5–6-GHz integrated receiver, this implies that an internally generated 10–12-GHz frequency (± the IF) is required for either high- or low-side LO downconversion. This signal is generated from a lower frequency source through the use of a monolithic frequency doubling circuit.

C. Frequency Doubler

There are a number of IC-compatible frequency doubling circuits available [14]–[17]. A new regenerative frequency doubling technique [18] is shown in Fig. 4. It is essentially a two-stage quadrature ring oscillator, which is coupled through C_c to an input signal (i.e., f_{in}). The fundamental frequency of the oscillator is synchronized to f_{in} by injection locking [19]. Each of the differential amplifiers is a simple emitter-coupled differential pair with resistive loads. The nonlinear characteristic of the differential pair produces a strong double-frequency component at the emitter-coupled node when the circuit is driven large-signal. At high frequencies (i.e., $>f_T/10$), the transistor parasitics attenuate higher harmonics so that the collector voltage is predominantly sinusoidal. The double-frequency ($2f_{in}$) differential signal is extracted across the emitter nodes of the two amplifiers in the ring [see Fig. 4(b)]. The "+" and "−" outputs are antiphase because the fully differential inputs to each amplifier stage are held close to quadrature phase (i.e., 0° and 90° phase, respectively) by the ring topology. Capacitive coupling at the input allows the oscillator to maintain a stable dc bias point through negative feedback and high dc gain. The common mode or fundamental component at f_{in} is suppressed from coupling efficiently to the output by the balanced topology.

Regenerative frequency doubling has a number of properties which make it suitable for monolithic integration. First, the output amplitude is almost independent of the input signal level. Also, regenerative circuits are power efficient and can provide substantial gain at high frequencies (approaching the transistor $f_T/2$). In addition, a very wide locking range (over an octave) is possible with low levels of input signal drive as the oscillator is locked in its fundamental mode rather than at a subharmonic. The low impedance outputs (at the emitters) have good signal-driving capability. The circuit is also relatively compact because inductors are not required. Finally, the output signal has low spurious content and does not require filtering, and multiplier stages can be cascaded to realize higher orders of multiplication without the need for interstage filtering.

Resistively loaded ring oscillators typically have a low Q-factor, and so a slight phase shift in the feedback loop can significantly alter the frequency of the oscillator from its natural frequency. When injection locked, the I and Q outputs of the oscillator are in quadrature (90° phase shifted) with a small phase error of approximately $<\pm 3°$. The magnitude of the phase error depends on the difference between the injected and free running frequency of the oscillator, the ring oscillator Q, and as a higher order effect, the injected signal amplitude. However, the I–Q outputs are not suitable for driving the mixers directly. This is because the phase error is too large for the image-reject mixer application, and the error is both frequency and gain dependent.

This error is a result of the imbalance introduced by signal injection, which adds or subtracts phase from the oscillation at only one stage [i.e., the first stage in Fig. 4(b)] of the ring. Signals at the emitter-coupled output nodes of the quadrature oscillator are therefore nearly 0° and 180° phase shifted (within approximately ±6°). Together they comprise a differential doubled-frequency output pair with a small common-mode signal component. For a 6° error, the common-mode signal is approximately 20 dB below the differential signal.

III. Circuit Description

The receiver RF IC is can be subdivided into two main blocks. The first block is the RF downconverter consisting of LNA, coupling transformer and balanced mixers (see Fig. 1). The remaining circuitry generates the quadrature (I–Q) LO signals needed to drive each mixer.

A block diagram of the subsystem used to generate the I–Q LOs used for downconversion is shown in Fig. 5. The first frequency-doubling stage is a four-stage ring oscillator that is injection locked to the LO input signal at a frequency of $f_{LO}/2$. The doubled-frequency differential output at f_{LO} is extracted from two emitter-coupled nodes at opposite (and quadrature) sides of the first stage (see the detailed schematic in Fig. 6). The f_{LO} differential signal is then fed to the next stage of frequency doubling via a buffering amplifier. This increases the injection-locking range of the second frequency doubler by increasing the amplitude of the injected signal. The buffer also improves the isolation between the two regenerative doubler stages and prevents the possibility of unintentionally locking the first stage to the second one.

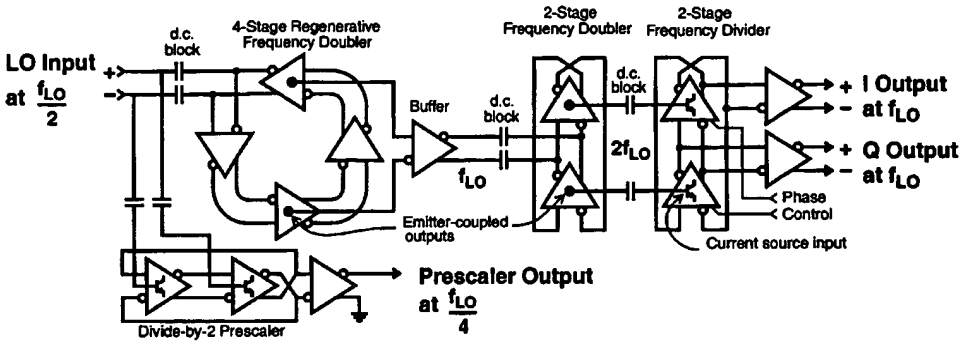


Fig. 5. I–Q LO subsystem.

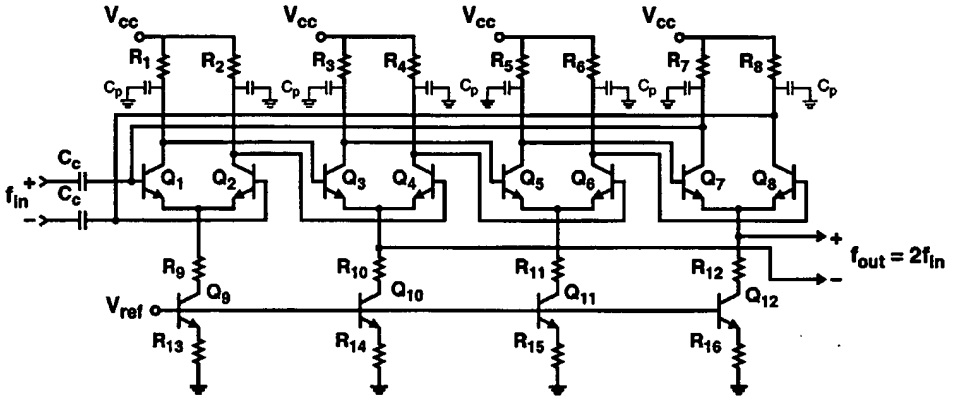


Fig. 6. Four-stage (first) frequency doubler.

A. First Doubler Stage

A schematic of the first frequency doubler circuit is shown in Fig. 6. Polysilicon resistors loads R_1 through R_8 are used in conjunction with their parasitic capacitances (C_p) to set the dominant pole for each amplifier in the ring. The parasitic capacitances (C_p) of the poly resistors vary proportionally with resistor area, thereby allowing their value to be controlled through layout. It should also be noted that resistors greater than minimum width are less susceptible to fabrication tolerances. Thus, the process variation of the resistors is reduced and explicit capacitor loads are not required. The use of a four-stage ring instead of a two-stage ring allows the doubled frequency signal to be extracted from the emitter-coupled nodes of $Q3$–$Q4$ and opposite pair Q_7–Q_8 rather than directly from the emitter-coupled node of the input transistors Q_1–Q_2. If a single-ended input source is used for injection, this topology will improve the suppression of the fundamental signal at the output due to the common-mode rejection ratio provided by the first stage (i.e., Q_1–Q_2). Resistors R_9–R_{12} increase the real output impedance of each bias current source at high frequencies and increases the common-mode rejection of each stage.

B. Second Doubler Stage

The second frequency doubler in the system (from Fig. 5) is implemented using a two-stage differential ring oscillator injection locked to f_{LO}. Its free-running frequency is centered at twice the free-running frequency of the preceding stage (i.e., ~5.5 GHz). This second stage of doubling provides an output at $2f_{LO}$ (or four times the input to the first doubling stage) when locked.

Fig. 7 illustrates the second frequency doubler in the LO subsystem. Two stages are used because a four-stage ring consumes excessive power and cannot operate at 5–6 GHz. Collector resistors R_1–R_4 are shown as segmented resistors in Fig. 7 to illustrate the distributed nature of parasitic capacitance C_p. In the 5–6-GHz band, parasitic reactances in the loads are low enough to affect performance and therefore an accurate estimate of the RC time constant for the load is necessary. With a single π-section to model the entire resistor, one-half of the total parasitic capacitance for each collector load is shunted to ac ground (V_{CC}). This gives an overly optimistic estimate of the loop gain for the ring oscillator and an incorrect free-running frequency. To avoid this, the parasitic capacitance is distributed across multiple π-sections, as shown in Fig. 7. For values less than 1 kΩ (as in this design), a series connection of three π-models is sufficient to model the effect of parasitic capacitance distributed along the resistor's length up to 6 GHz.

In order to increase the loop gain of the oscillator, the dominant pole of the amplifying stages is set as high as possible by reducing the parasitic capacitance at the collector nodes, while additional (and much needed) phase lag is introduced in the feedback path of the loop of the oscillator using an RC delay line consisting of resistors R_5–R_8. Low-pass filtering caused by the

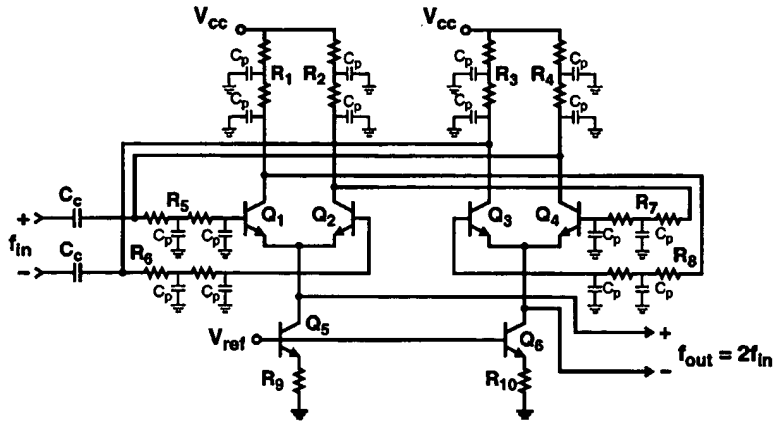


Fig. 7. Second-stage regenerative frequency doubler.

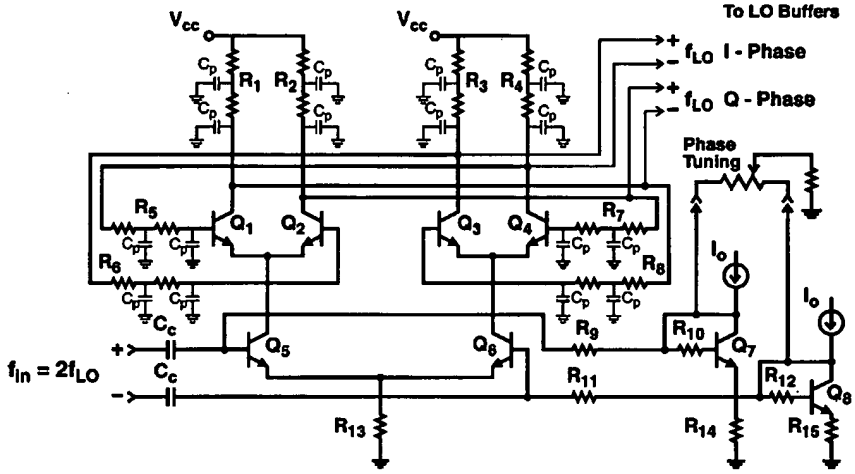


Fig. 8. Frequency divider with I–Q outputs and phase tuning.

parasitic capacitance of these series-connected resistors (which is determined by their area) lowers the free-running frequency with little degradation in the loop gain.

C. I–Q Regenerative Divider and Prescaler

Again referring to Fig. 5, the $2f_{LO}$ signal provided by the second doubling stage (at ~10–12 GHz) is divided into accurate I and Q signals by a two-stage regenerative frequency divider. The two-stage doubler and two-stage divider used here are virtually identical ring oscillators running at the same fundamental frequency (~5–6 GHz). The two circuits are coupled by the input differential pair to the divider (Q_5 and Q_6 in Fig. 8). The two-stage doubler (Fig. 7) is asymmetrically driven, leading to small I–Q phase errors (less than approximately 3°). However, the divider is symmetrically driven by a $2f_{LO}$ signal injected differentially into its emitter-coupled nodes. Due to this symmetry, the I and Q outputs of the divider remain in quadrature (i.e., 90° phase-shifted), with an error of less than 1°.

Fig. 8 shows a schematic diagram of the frequency divider used to generate I and Q LO signals for the downconverting mixers. The circuit consists of cascaded differential amplifier stages in a ring oscillator configuration. Differential pair Q_5–Q_6 converts the $2f_{LO}$ input voltage to a differential current which synchronizes the ring oscillator (Q_1–Q_4) to the input signal. The input differential pair (Q_5–Q_6) also isolates the divider from the preceding stages. Resistors R_9 and R_{11} isolate the 2LO input from the parasitics of bias transistors Q_7 and Q_8. The divided I and Q outputs at f_{LO} are buffered by differential amplifiers and then ac coupled to the inputs of the mixer quads.

The time delays through each stage of the divider are well matched, resulting in quadrature output signals with less than 1° of phase error throughout its frequency locking range, which is approximately one octave. By disturbing the symmetry of the ring oscillator in a controlled manner, the phase angle between I and Q outputs can be altered. Since the frequency of the oscillator is fixed by the injection locking of the circuit to the $2f_{LO}$ input signal, only the phase relationship between the outputs can be changed. Note that the amplitude is determined by the maximum output swing of the differential amplifier stages. In this way, the phase relationship between I and Q LO outputs is tuned. A convenient way of adjusting the symmetry of this circuit is to (differentially) alter the bias currents of Q_5 and Q_6. This increases the phase delay of one output of the input pair

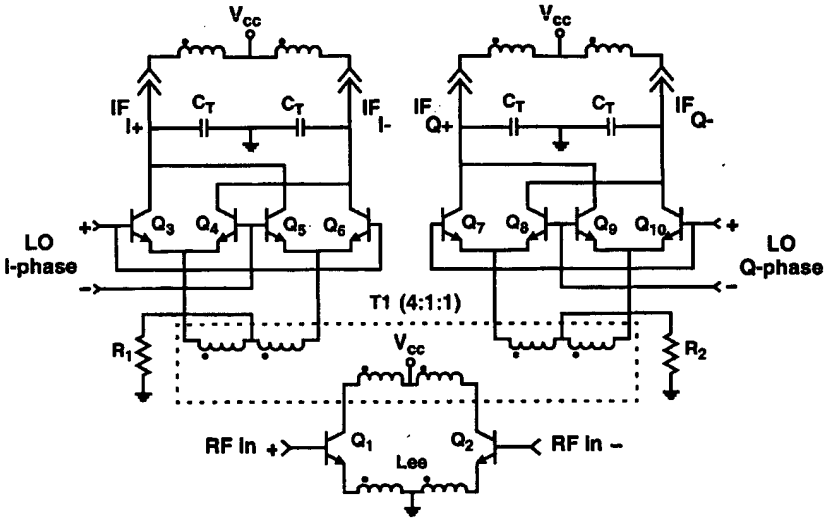


Fig. 9. RF downconverter schematic diagram.

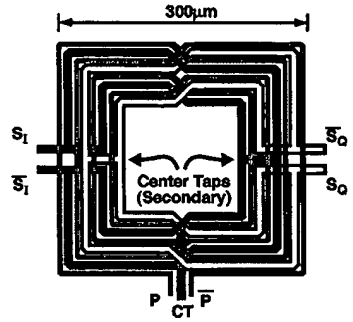
while reducing delay through the other. Note that diode-connected transistors Q_7 and Q_8 (shown in Fig. 8) bias each stage of the divider. The bias currents through Q_5 and Q_6 are therefore isolated from each other but are referenced back to a common reference source (I_o). The simple potentiometer shown in the figure illustrates how the bias currents (and hence I–Q phase) were altered in testing. It is proposed that this method of phase control could be implemented monolithically with a simple current-biasing digital-to-analog converter.

The prescaler is identical to the frequency divider shown in Fig. 8 except that the component values are altered to lower free-running frequency to $f_{LO}/4$. Note that for the prescaler, only one of the divider outputs is required. The output of the prescaler is buffered by an open collector differential amplifier, which consumes 4 mW of power.

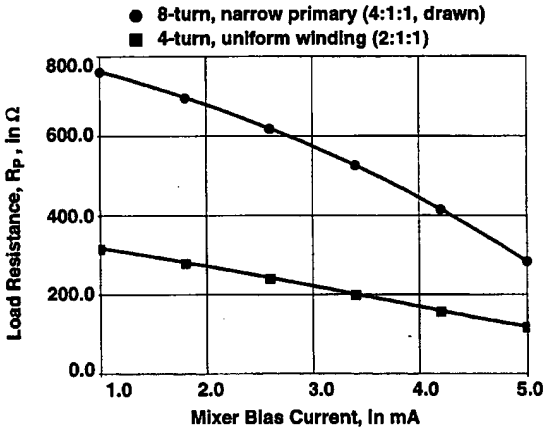
D. RF Downconverter

A complete circuit schematic of the RF signal path is shown in Fig. 9. The off-chip matching, bias and quadrature-combining networks at the IF ports used in testing and evaluation of the IC performance are not shown on the schematic for simplicity. Parasitics for the 32-pin package were accounted for in the design. The topology used for the RF section is similar to that described in [5], [6], however, there are significant differences in this design. First, a new fully monolithic interstage coupling transformer with a noninteger turns ratio is designed to increase the overall preamplifier gain and improve coupling efficiency. Also, given the narrow operating margin for the receiver in this technology (i.e., f_T/f_{RF} is less than 5), the transistor sizes, degeneration inductance, and transformer parameters are carefully selected to maximize dynamic range (i.e., minimum noise figure with a high input intercept), improve the input match, and minimize power consumption in a standard IC package.

T_1 is a fully symmetric monolithic transformer design [20] which acts as an interstage coupling circuit and also feeds dc bias to the LNA and mixers. In order to realize 15-dB LNA gain above 5 GHz with a few milliamperes of bias current, the impedance reflected from the secondary to the primary winding of the transformer must be on the order of 300–400 Ω per side. This was realized by designing a noninteger turns ratio transformer with minimal parasitic loading. The shunt parasitics ap-



(a)



(b)

Fig. 10. Monolithic transformer. (a) Physical layout. (b) Resistance seen at the primary (f = 5.5 GHz).

pear in parallel with the reflected impedance, thereby limiting the impedance seen at the primary terminals. The turns ratio is 4 : 1 : 1 as drawn in the physical layout [see Fig. 10(a)]. However, the primary winding has a narrower line width than the secondaries, which results in a step-up factor in addition to the geometric turns ratio. The final design consists of eight turns of 5 and 10-μm-wide Al top-level metal with a metal-to-metal spacing of 3 μm, measures 300 μm on a side, and has three ports: one on the primary (LNA) side and two for the mixing quads. DC bias is fed to the LNA and mixer circuits via the center taps. A program written to simulate the behavior of arbitrary configurations of microstrip lines on silicon [21] was used to extract a SPICE model for the transformer, which was used in circuit simulations of the RF path.

The doubly balanced mixers (Q_3–Q_{10} in Fig. 9) consist of four-transistor Gilbert-type switching quads. The impedance seen at the common-emitter side of the switching quad is proportional to the transconductance of bipolar junction transistors (BJTs) in the quad. Hence, the bias current is selected to provide the desired load impedance for the preamplifier when reflected from secondary to the primary side of the transformer. The load resistance at the transformer primary as a function of the mixer bias current is plotted in Fig. 10(b). A resistance less than 300 Ω is seen at the primary for a 2 : 1 : 1 turns ratio design (four turns of 8-μm-wide top-level metal with a metal-to-metal spacing of 2.8 μm, measuring 275 μm on each side). The load impedance increases to above 600 Ω when the geometric turns ratio is increased (i.e., 4 : 1 : 1 layout) and a narrower width primary winding are used. However, the improvement is less than predicted by the change in turns ratio (due to parasitic losses) and is limited to about a factor of three.

The preamplifier stage consists of transistors Q_1 and Q_2 (from Fig. 9), which are driven differentially from the RF inputs. Differential drive improves the Q-factor of the trifilar transformer and emitter degeneration inductor by approximately 50% [22]. Also, the preamplifier is designed so that an impedance match at the RF input realizes both minimum noise figure and maximum power transfer for the stage for the load impedance seen at the transformer primary. A simultaneous matching procedure employing both series feedback from the emitter via inductor Lee and shunt feedback via the collector–base (i.e., Miller) capacitance is used [6]. An emitter area of 20 × 0.5 μm^2 was selected after careful optimization including all parasitic effects. For 5–6-GHz operation, simulations predicted that a noise figure of 2.2 dB and gain of 15 dB is realizable at a bias current of 2.5 mA per transistor and Lee = 0.8 nH, with a coincident noise and power match at the input.

IV. Experimental Results

The test IC was packaged in a 32-pin ceramic quad flatpack (CQFP) and mounted in a custom test fixture for evaluation, using the configuration shown in Fig. 11. The RF and LO signals are delivered to the IC differentially via 50-Ω microstrip lines. Losses for the RF input signals (including connectors) in the fixture are approximately 1 dB.

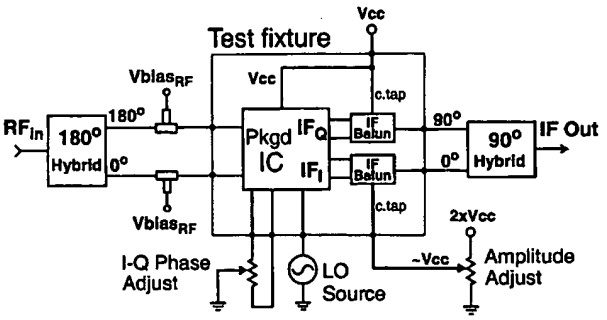


Fig. 11. Experimental test configuration.

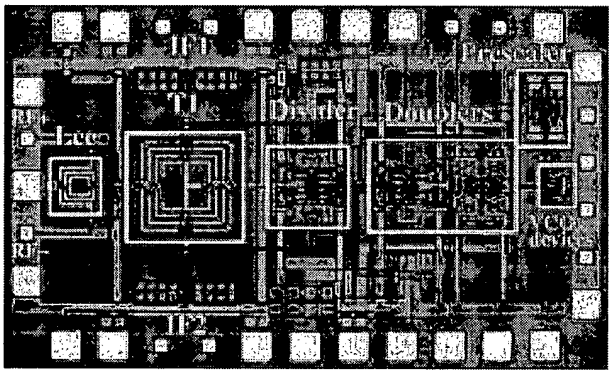


Fig. 12. Photomicrograph of the receiver IC.

A photomicrograph of the receiver RF IC is shown in Fig. 12. The main circuit blocks are highlighted and annotated on the figure. The overall die size is 1.9 × 1.2 mm^2, which includes the bonding pads. The active area is considerably smaller, as extra bondpads were added to aid in testing. Substrate coupling between the multiplier, divider, mixer, and LNA circuits is minimized through component separation in layout, separate supply bussing and the use of grounded p+ diffusion guard rings to isolate the various blocks. This, in addition to the use of fully differential RF, LO, and IF signals, results in greater than 60 dB of isolation for the packaged device in the test fixture.

Discrete transformer baluns with a 4 : 1 turns ratio are used to present a differential impedance of approximately 800 Ω at the open-collector mixer outputs of the test chip. The IF baluns have a minimum loss of 1.3 dB at 75 MHz, thereby restricting the IF used for measurement. A lower turns ratio discrete balun operates at a higher IF but with a lower impedance transformation, which reduces the overall conversion gain. To compensate for parasitic losses and mismatches, a three element matching network was designed to match the balun output to the (50 Ω) quadrature IF combiner of Fig. 11.

As can be seen in Fig. 11, potentiometers are used to adjust the amplitude (via the supply voltage of one of the mixers) and phase (via bias current of the quadrature LO frequency divider) in the I and Q paths to maximize the image rejection. It is proposed that in a real application, these controls would be set during a self-calibration period upon startup or during idle times. A digital or analog tau-dither-type feedback circuit

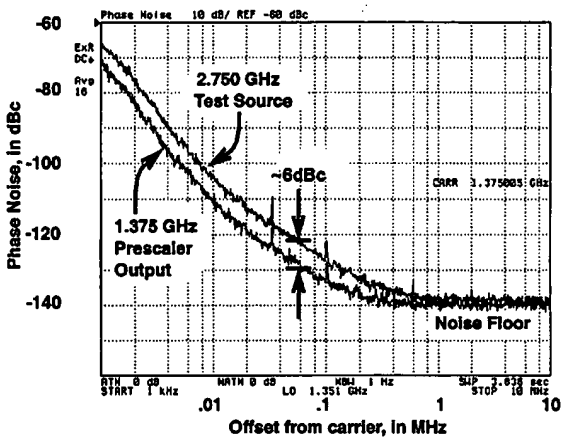


Fig. 13. Measured single sideband phase noise of the prescaler. $V_{CC} = 2$ V.

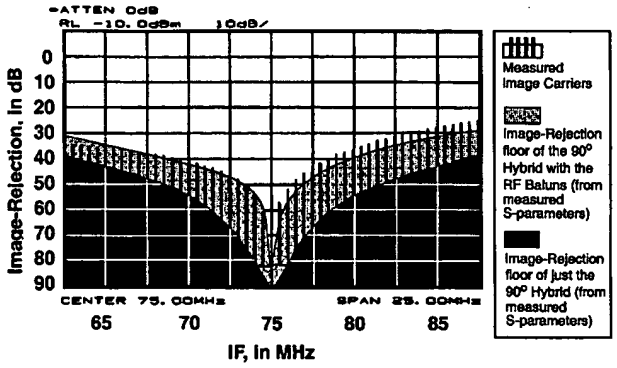


Fig. 14. Measured image rejection for a 75 MHz IF (test set-up of Fig. 11).

[23] could alternately adjust phase and amplitude controls for maximum rejection of an internally generated test carrier in the image band (e.g., generated by the transceiver's up-converter). The received signal strength indicator (RSSI) found in most demodulator systems could be used to measure image-rejection during calibration. The phase errors in the LO were measured at less than 0.011° (as inferred from the measured image rejection) by manually following this routine. This level of I–Q accuracy cannot be achieved without the use of trimming, tuning, or self-calibration techniques.

The entire chain (multipliers and divider) is locked from a −18 dBm input (LO) signal source over the frequency range of 1.9 to 3.2 GHz, which in turn generates I and Q output signals for the mixers in the range from 3.8 to 6.4 GHz. The 4 × LO frequency range that is generated and fed to the mixer divide-by-two is 7.6 to 12.8 GHz, which is greater than one-half of the 25-GHz transistor unity gain frequency. This very high fraction of f_T is achieved through the use of regenerative circuits. The power dissipation of the entire LO subsystem (excluding the optional LO prescaler) is 44 mW from a 2.2-V supply. All undesired harmonics, including the fundamental ($f_{LO}/2$) input, are suppressed by over 30 dBc in the f_{LO} output for single-ended excitation, and by more than 35 dBc for a differential input source.

It should be noted that the power dissipation of the LO system reported here is 11 mW higher than the 22 mW reported in [18]. The receiver IC was modified to lower the center frequency and broaden the locking bandwidth. This increase in power affords an increase in the relative locking bandwidth from 26% (previously) to over 50%. The added margin may not be necessary for a 5–6-GHz receiver application, but it clearly illustrates the ability to achieve a very wide operating range using injection-locking techniques.

The prescaler dissipates 1.5 mW from a (minimum) 1.5-V supply and remains locked over an input frequency range of 600 MHz to 4.0 GHz (for a −6 dBm LO input signal to the IC). It should be noted that this type of regenerative divider does not have any other dominant modes of division (other than divide-by-two) and so unpredictable mode locking to unwanted harmonics is not a concern.

The single sideband phase noise of the prescaler output is plotted in Fig. 13. A supply voltage of 2.2 V (4.3-mW power dissipation in the prescaler) is used for the measurement. This is consistent with the bias conditions for the other injection-locked circuits in the LO system. The phase noise of the divider output closely follows the theoretical 6-dB improvement compared to the phase noise for the input source predicted for an ideal divide-by-two. The noise floor of the analog divider is less than −140 dBc (i.e., noise floor of the test instrument) with no spurious components. From this result, it can be inferred that the I and Q outputs at f_{LO} driving the downconverting mixers have close to 6 dB greater phase noise than the $f_{LO}/2$ input carrier (the theoretical minimum), since the analog regenerative technique used for frequency dividing in the prescaler is also used for frequency doubling and dividing in the LO chain.

The measured image rejection (IR) over a wideband using a discrete 90° quadrature IF combiner centered at 75 MHz is plotted in Fig. 14. The black-shaded IR floor (i.e., lower bound on IR) shows the lowest possible IR for the 90° external IF combiner employed in the test setup. This floor was calculated from s-parameter measurements of the combiner, which characterize its frequency dependent phase and amplitude variations. Prior to computing the maximum IR, systematic phase and amplitude offset errors are subtracted from the measured parameters to center the maximum rejection at 75 MHz, thereby simulating an ideal trim of phase and amplitude errors. The grey-shaded region in Fig. 14 shows the lowest possible image rejection when the s-parameters of the IF combiner, transformer baluns, and matching stages are considered. The vertical lines are actual measurements of the image suppression, showing the wideband performance achieved experimentally. A maximum IR of approximately 80 dB is obtained at the 75-MHz center frequency. This implies that a phase-tuning precision of better than 0.01° is achieved by adjusting I–Q phase relationship via the frequency divider stage. Also, the measured IR is within ±5 dB of the maximum IR predicted for this test setup. Discrepancies between the measured and expected results (i.e., vertical lines and the grey-shaded region) are likely due to component variations. The grey-shaded region is estimated for s-parameters of a single transformer balun and does not account for variations between the two baluns and matching networks actually used in the experimental setup.

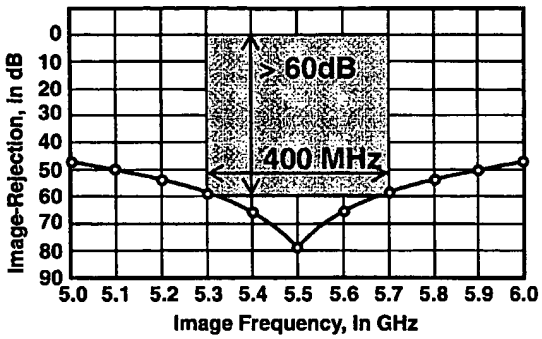


Fig. 15. Image rejection across the RF band for a swept RF LO. IF = 75 MHz.

TABLE I
SUMMARY OF EXPERIMENTAL MEASUREMENTS

Parameter	25 GHz f_T Silicon Bipolar			45 GHz f_T SiGe [ref. 5]
RF Input, GHz	5.3	5.8	5.5	5.8
VCO Input Frequency, GHz	2.6875	2.9375	2.7875	5.55 (no VCO)
IF, MHz	75			250
Supply Voltage, V	2.2		2.34	1.8
Conversion Gain, dB	15.1	14.9	17.0	14.2
Input IP3, dBm	-9.4	-10.5	-4.5	-5.9
RF Input Return Loss, dB	14.0	14.6	14.3	(wafer probe)
SSB Noise Figure (50Ω), dB	5.1			6.8
LO to RF Isolation, dB	60			63
Maximum Image Rejection	80dB (tuned at center of IF) Implies 0.01° precision in phase			36.5 dB
Power Dissipation, mW	44.4		55.0	18.5

A measurement of the image rejection was also performed with a constant IF of 75 MHz. The purpose of this test is to measure the phase and amplitude variations of the I and Q LO outputs driving the mixers as a function of the LO frequency. In order to do this, the RF and LO frequencies are swept together across the 5–6-GHz band maintaining a constant frequency difference of 75 MHz between them. The phase and amplitude of the LO is trimmed only once for maximum IR with an RF input at the center of the 5–6-GHz band (i.e., 5.5 GHz) prior to beginning the sweep. As shown in Fig. 15, this results in an image rejection of nearly 80 dB. As the RF (and LO) is swept away from 5.5 GHz, the image rejection decreases because of increasing phase and amplitude errors in the quadrature LOs, however, between 5.1–5.8 GHz the IR is maintained at better than 50 dB without retuning. The results of this test infer that the phase variations in the LO are less than 0.064° over a 1-GHz sweep.

Table I lists a summary of the measured results of the receiver's performance. An IF of 75 MHz was used. It should be noted that the IF is not restricted by the receiver topology. The RF input is unmatched externally, however, an input return loss >-14 dB was measured across the receive band. The minimum conversion gain measured for the receiver is approximately 15 dB across the 5.3–5.8-GHz band, which is close to the design value. A relatively low overall single sideband noise figure (50 Ω) of 5.1 dB was measured along with an input third-order intercept of −9.4 dBm, giving the receiver a wide dynamic range despite the low supply voltage (2.2 V) and bias current (10 mA) used for the LNA and mixers. These results compare very favorably with those reported for similar designs in the same technology at 1–2 GHz as well as other 5–6-GHz designs [8], [24]–[26].

A significant improvement in both gain and linearity is realized when the supply voltage is raised from 2.2 to 2.34 V. This is due to the larger LO signal drive presented to the mixer quads as a result of increased voltage headroom. At 2.34 V, the conversion gain rises to 17 dB and the input intercept point (IIP3) improves by 5 dB to −4.5 dBm, while the noise figure is unchanged.

V. CONCLUSION

A 5–6-GHz image-reject receiver IC is implemented in a 0.5-μm 25-GHz silicon bipolar technology that draws just 22 mA from a 2-V supply. The image rejection obtainable with this IC (up to 80 dB) is sufficient to eliminate the off-chip interstage RF filter in a heterodyne receiver, thereby simplifying packaging requirements and decreasing costs. New methods of regenerative frequency doubling, I–Q phase error compensation, and RF interstage coupling make this design possible. Low-voltage circuit topologies are used throughout to minimize power consumption and ensure compatibility with deep-submicron CMOS (baseband) application-specific integrated circuits (ASICs) operating from low-voltage supplies. The wide dynamic range and low power consumption of this receiver IC demonstrates that silicon technology is capable of addressing the requirements for RF interfaces in emerging applications at 5–6 GHz.

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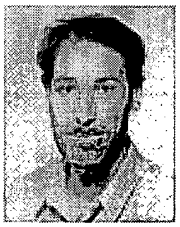

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Dr. Long was the recipient of the 1997 Natural Sciences and Engineering Research Council of Canada (NSERC) Doctoral Prize and the Douglas R. Colton and Governor General's Medals for research excellence at the Ph.D. level.

Patent Supplimental Information

Attached January 31/01

by James Maligeorgos

Table of Contents

List of Figures

1) On the Injection Locking of Multi-phase or Ring Type Oscillators.

In this paper, the injection locked ring oscillator (ILRO) is examined. A simple Simulink model of the system is developed and validated through comparisons to HSPICE simulations of the same circuit to provide useful insight into some of the fundamental characteristics of the ILRO. Finally, some uses for an injection locked ring oscillators are also described.

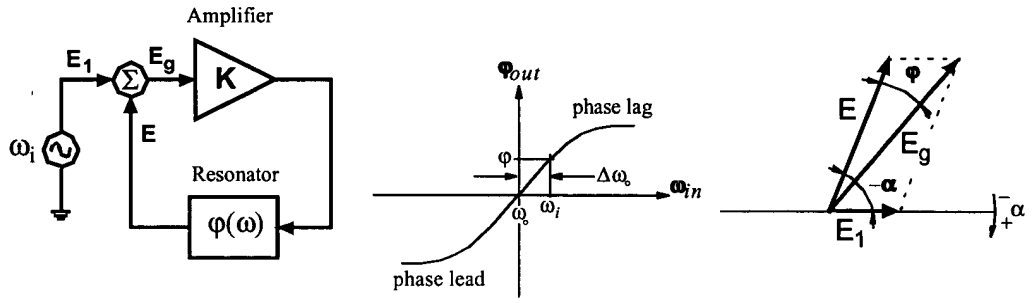
1.1 Fundamental Characteristics of Injection Locked Oscillators.

The injection locking of a single-phase type oscillator is well known in the state of the art of electronics[38]. Due to the unique mechanism of oscillator synchronization, it is well known that most injection locked oscillators (ILOs) share some basic characteristics. (For a full derivation of the relationships used in this section, please refer to Appendix A.)

Shown in Figure 1.1a is a simple model diagram of an ILO. The necessary condition required to lock the oscillator can be expressed as

$$\frac{E_1}{E} > 2Q\left|\frac{\Delta\omega_o}{\omega_o}\right|, \tag{1.1}$$

where Q is the quality factor of the oscillator, ω_0 is the free-running frequency of the "undisturbed" oscillator, and where $\Delta\omega_0$ is the difference between the frequency of the injected signal (ω_i) and ω_0. E_1/E is the ratio of the injected signal amplitude to the oscillator's amplitude at the summing node as depicted in Figure 1.1a. Figure 1.1b illustrates an example oscillator resonator phase response.



a) Simple oscillator b) Resonator phase response c) Phasor diagram

Figure 1.1 Injection locked oscillator model

From equation 1.1, some of the fundamental properties of an ILO can be stated. For a given level of injected signal drive (E_1), we see that an ILO will have a finite band of frequencies ($\Delta\omega_0$) centered around its free-running frequency ω_0, over which it is able to become locked. The ratio of $\frac{\Delta\omega_o}{\omega_o}$ can also be stated as the relative locking bandwidth of the oscillator and is typically expressed as a percentage. This relative locking bandwidth is proportional to the ratio of $\frac{E_1}{E}$ and inversely proportional to the Q of the oscillator. This implies that an infinitesimally small level of injected signal is required to lock the oscillator at it's free-running frequency ($\omega_i=\omega_0$), and that very high-Q oscillators cannot be locked over a wide frequency range without an increased injection amplitude.

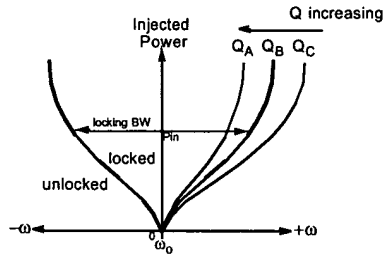


Figure 1.2 Typical locking range of an ILO

The typical locking characteristic of an ILO as a function of injected power is plotted in Figure 1.2 for illustration.

When an oscillator becomes synchronized to an external input signal, there is a static phase relationship between the input signal and the oscillator. The oscillator becomes 'locked' in both frequency and phase to the input signal. The steady state phase relationship between the injected signal and the oscillator is depicted in Figure 1.1c and can be expressed, under the assumptions stated in the Appendix, as

$$\sin\alpha = 2Q\frac{E}{E_1}\cdot\frac{\Delta\omega_o}{\omega_o}. \tag{1.2}$$

This implies that if the oscillator is locked at its free-running frequency there is no phase shift between the injected signal and the locked oscillator. As the forced oscillator approaches the edge of it's locking range, the phase shift between the injected signal and the oscillator approaches 90°. This is the angle at which the oscillator finally becomes unlocked and beyond which the oscillator runs freely.

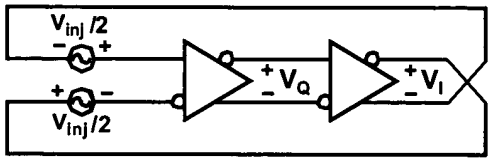
One of the most useful features of an injection locked oscillator, is that since the oscillator is locked to the phase of the input signal, the phase noise properties of the injecting source are preserved by the locked oscillator. Thus if an oscillator with a poor free-running phase noise characteristic becomes locked to a very high quality (low-phase noise) injection source, the phase noise of the locked oscillator will also be low since it will track the phase of the input source very closely.

1.2 Injection Locked Ring Oscillators

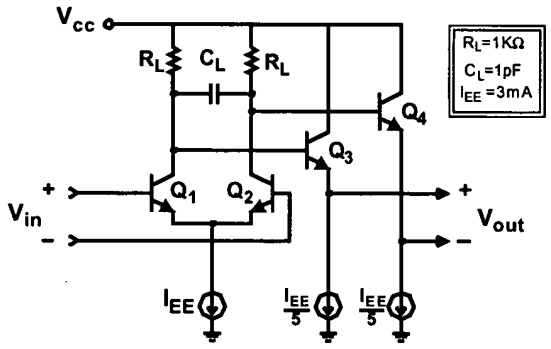
Although there exist many different types of oscillator topologies in the state of the art, most injection locking techniques have been realized using oscillators of the single-phase type only[33]. The author is unaware of any examples in the literature which describe the injection locking of a multi-phase type oscillator, such as a ring oscillator, in its fundamental mode. In this section, the fundamental mode locking of a quadrature ring oscillator with resistive loads is studied. An appropriate model to explain its operation and characteristics will be compared with some simulated results.

In order to simplify the analysis, we will assume that the injected signal can be ideally summed in the feedback path of the oscillator as illustrated in the topology of Figure 1.3a.

The schematic diagram for the differential amplifiers is shown in Figure 1.3b.



a) Block diagram showing ideal injected signal summation



b) Differential amplifier realization

Figure 1.3 Injection locked ring oscillator topology

It is obvious to anyone in the art that a multi-phase or ring-type oscillator topology is not limited to two amplifying stages in the ring and that the amplifying stages of the ring can be realized with almost any type of amplifying circuit including simple logic inverter gates.

In order to simplify the analysis of the ILRO topology described in Figure 1.3, the R-C-R load of Q_1 and Q_2 are chosen to dominate the transistors' collector node parasitics and emitter followers Q_3 and Q_4 are employed to isolate the loading of the next stage from the current stage.

The differential output current for the emitter-coupled transistor pair Q_1 and Q_2 of Figure 1.3b can be expressed as[35]:

$$I_{od} = \alpha_F \frac{I_{EE}}{2} \cdot \tanh\left(\frac{-v_{id}}{n V_T}\right), \tag{1.3}$$

where α_F is the dc common-base current gain, $v_{id} = v_{in}$ of Figure 1.3b, I_{od} is the differential output current across the collectors, n is an ideality factor depending on process parameters, and $V_T = kT/q$ is the thermal voltage of the transistors.

HSPICE Simulations were used to parameter fit $n = 1.51$, and $\alpha = 0.98$ of equation 1.3 to a differential-pair of 0.5um x 10um emitter area transistors in a 25GHz f_T process (for I_{EE} = 3mA). The dominant pole for the amplifying stage can be determined from the first-order solution of the RC load giving

$$f_{p1} = \frac{1}{2\pi \cdot 2k\Omega \cdot 1pF} = 79.6MHz. \tag{1.4}$$

The choice of R_L and C_L for this model were chosen intentionally to set the free running oscillation frequency to approximately 1GHz (i.e. 1/25 f_T) such that parasitic effects of the transistors would not dominate the analysis as they would at higher oscillation frequencies.

A simple first-order approximation of each stage is not sufficient since the higher-order parasitics of the transistor add significant phase shift. In addition, the phase shift of a first order network will only approach 90° for frequencies $\omega \gg \omega_{p1}$ and will never reach or surpass it, (see equation 1.5). Since the Barkhausen[39] criterion requires that the two amplifying stages in the oscillator contribute a total of at least 180° of phase shift for oscillation to occur; each amplifying stage of Figure 1.3 must be approximated by at least a second-order system.

$$\tan^{-1}\left(\frac{\omega}{\omega_p}\right) = \theta_p \tag{1.5}$$

$$\theta_{p1} + \theta_{p2} = 90° \Big|_{\omega = 2\pi f_{osc}} \tag{1.6}$$

HSPICE simulations show that the oscillator will have a free running frequency of 898MHz and an amplitude of 340mVp. Using this free-running frequency, equations (1.4), (1.5) and (1.6), can be used to back calculate an equivalent second pole for each amplifying stage in the simulink model to achieve the required 90° phase shift at 898MHz; resulting in f_{p2}=10.13GHz.

A Simulink (Matlab) model of the ring oscillator having the topology of Figure 1.3a with the modeled amplifiers of Figure 1.3b is shown in Figure 1.4 along with its associated parameters. In this oscillator model there are two critical variables (f_{p1} and f_{p2}). There are also two optimization goals for the model: The oscillator's free-running frequency and it's output amplitude. The HSPICE circuit simulator predicts that the circuit should have a free-running frequency of f_{osc}=898MHz and an oscillator amplitude of $Aosc$=340mVp. The original calculations of f_{p1}=79.6MHz and f_{p2}=10.13GHz results in f_{osc}=959MHz and $Aosc$=295mVp in the Simulink mathematical model solver. This is represents a +3.3% frequency error and -1.2dB amplitude error compared to HSPICE. The amplitude of the oscillator is expected to decrease with increasing frequency, as will be discussed shortly, and so the polarity of the amplitude error is found to be consistent with the polarity of the frequency error. A possible explanation for the positive frequency shift might be that the higher order frequency components generated by the *tanh* function of the transistor large-signal equation, although small, have a non-negligible effect on the zero-crossing of v_{id} leading to an unexpected phase shift at the oscillator's fundamental frequency.

Manual optimization of the pole frequencies in the Simulink model to f_{p1}=78MHz and f_{p2}=9.0GHz achieves < 0.3% frequency and amplitude error compared to HSPICE simulations of the oscillator in the free-running condition.

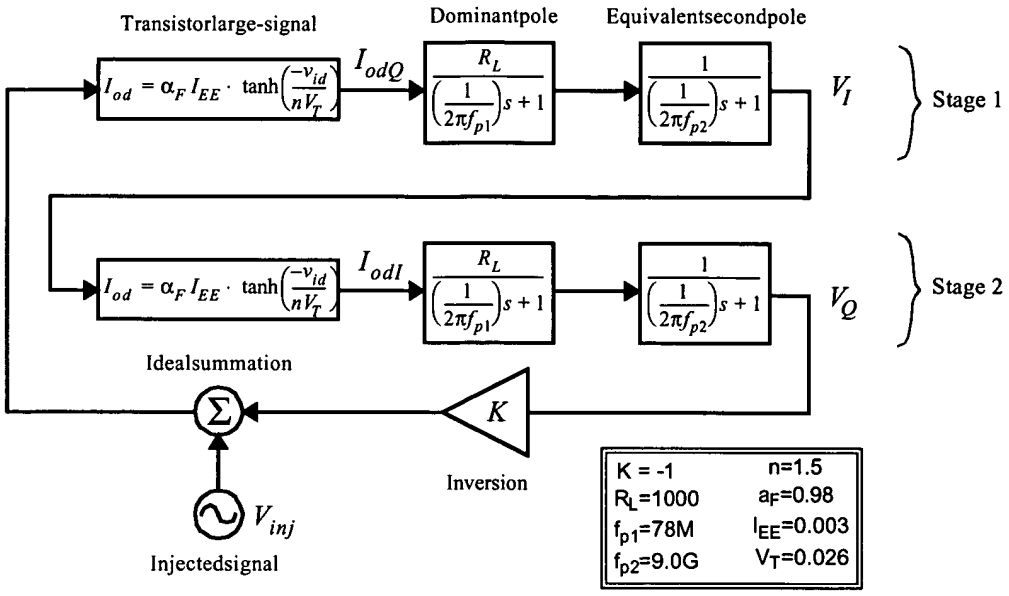


Figure 1.4 Simulink model of the ring oscillator in Figure 1.3

1.2.1 Matlab Simulink Model versus HSPICE Simulation

Two critical measurements of an injection locked oscillator are the output amplitude as a function of frequency and the locking range as a function of injected signal level. The output amplitude is measured differentially across the quadrature (V_Q) nodes as labeled in Figure 1.3a. Figures 1.5 and 1.6 show the output amplitude and locking range as a function of frequency for both the HSPICE simulations and the Simulink model. Both are in very close agreement for locking frequencies below 1.3GHz (or 50mVp injection level).

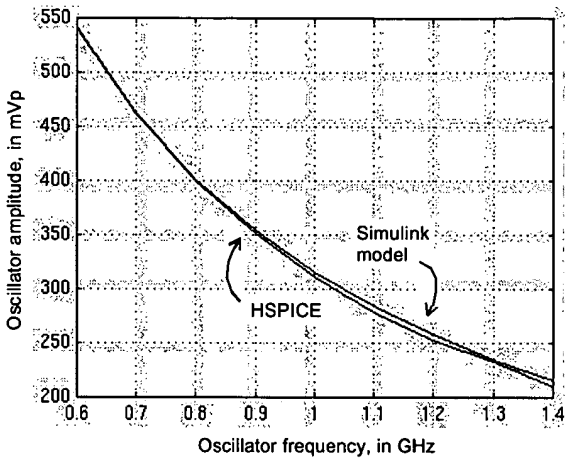


Figure 1.5 Oscillator Amplitude - HSPICE vs. MATLAB

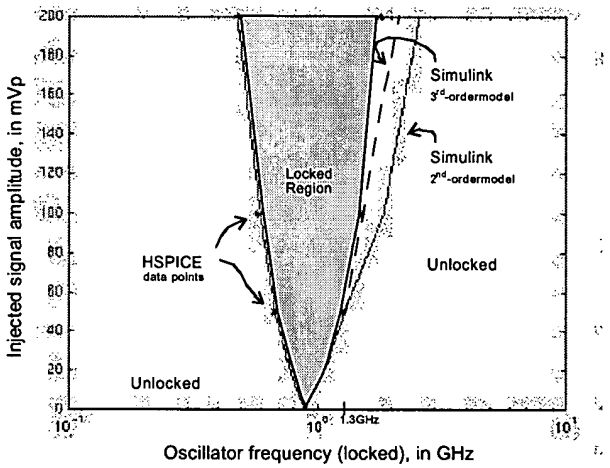


Figure 1.6 Locking range - HSPICE vs. MATLAB

With the injection level increased to 100mVp, the Simulink model predicts that the upper bound of the locking range is now 1.8GHz. HSPICE simulations, however, show an unusual phenomenon above 1.5GHz, whereby the fundamental locking mode of the oscillator is lost and the oscillator begins to act as a frequency halver (divide-by-2 circuit). It was hypothesized that this phenomenon might be caused by the higher-order poles of the active devices in the HSPICE simulation which are not being accounted for in the Simulink two-pole amplifier models in Figure 1.4. A third pole was introduced into each amplifying half of the

oscillator (Figure 1.7) to attempt to validate this hypothesis. Simulations indeed verified that the frequency halving effect at frequencies above 1.5GHz in HSPICE, are captured accurately in simulink by introducing a third pole into the model at an empirically determined frequency of $f_{p3} = 21.45GHz$. Figure 1.6 includes a curve showing the improved correlation between the locking range obtained by the third-order simulink model and the HSPICE simulated results.

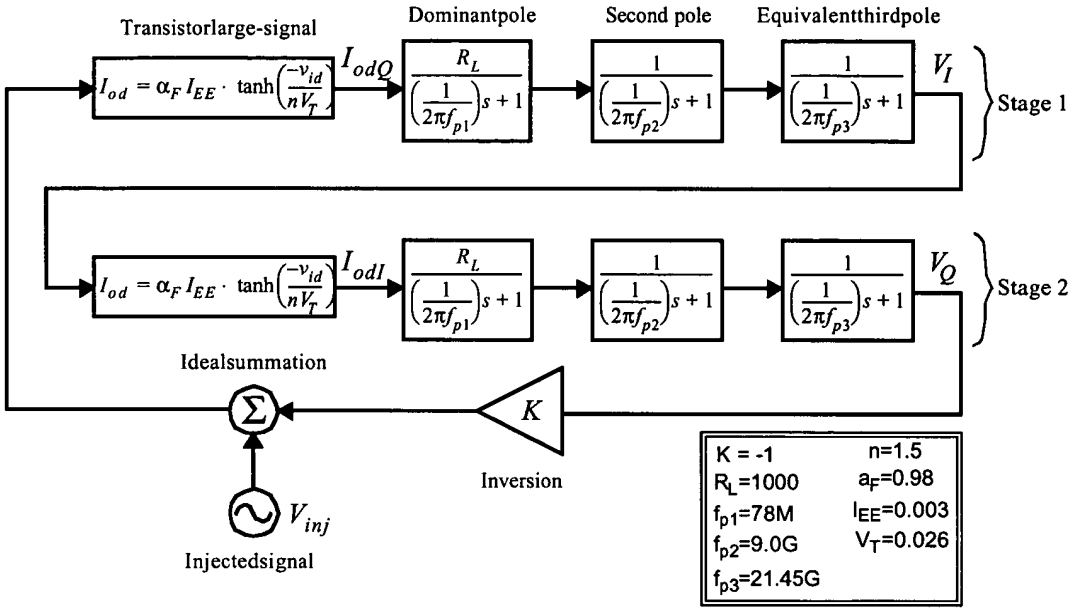


Figure 1.7 An ILRO model using a three-pole amplifier model

Increasing the injection level further still, to 200mVp, causes the oscillator to be able to remain locked to even higher frequencies. Under this condition, the third-order Simulink model now describes the frequency-halving effect to occur at 1.8GHz. The HSPICE simulation however, now shows halving to occur at a higher frequency of 2.2GHz. Although only two poles are required to characterize the lower end of the frequency locking range, an increasing number of poles (and zeros) are found to be required to model the system at higher and higher frequencies. This suggests that at the high frequency end, the device parasitics begin to strongly influence the oscillator's behaviour, and that at the low frequency end the higher-order effects can be neglected.

1.3 ILRO Model Observations

There are some basic observations that can be made directly from the simulink model. Only the two-pole model of Figure 1.4 is considered for simplicity. The amplitude, for instance, is dominated by the low frequency pole f_{pl}. An injection locked ring oscillator having RC loads will therefore have an amplitude vs. frequency curve that follows a first-order (-6dB per octave) response.

The phase response of a single amplifying stage in the oscillator is shown in Figure 1.8. The free-running frequency is expected to occur where the phase shift per stage is 90°. For a second order system, this occurs at the geometric mean of the two poles,

$$\omega_o = \sqrt{\omega_{p1}\omega_{p2}} \ . \tag{1.7}$$

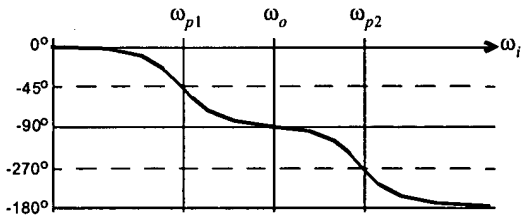


Figure 1.8 Differential amplifier phase shift

Figure 1.8 also shows that between ω_{p1} and ω_{p2}, the slope of the phase response is a minimum at ω_o, which means that the oscillator requires a minimal amount of phase change to alter the frequency of oscillation. This translates to a wide locking range according to equation 1.1.

The slope of the phase response (for both amplifier stages) at the free-running frequency can be determined using

$$\phi(\omega) = -2\tan^{-1}\left(\frac{\omega}{\omega_{p1}}\right) - 2\tan^{-1}\left(\frac{\omega}{\omega_{p2}}\right) \ , \tag{1.8}$$

and

$$A = \left.\frac{d\phi}{d\omega}\right|_{\omega=\omega_o} = -\frac{2/\omega_{p1}}{1+\left(\frac{\omega_o}{\omega_{p1}}\right)^2} - \frac{2/\omega_{p2}}{1+\left(\frac{\omega_o}{\omega_{p2}}\right)^2} \quad . \tag{1.9}$$

Combining equations 1.7 and 1.9, and by letting

$$k = \omega_{p2}/\omega_{p1}, \tag{1.10}$$

gives

$$A = \frac{-4\sqrt{k}}{1+k} \cdot \frac{1}{\omega_o} \quad \text{, or} \tag{1.11}$$

$$A = \frac{-4}{\omega_o\sqrt{k}} \qquad (\text{for } k \gg 1). \tag{1.12}$$

For comparison with the general definition of the Q-factor of an RLC tank based oscillator, we can say that the Q-factor for a 2-stage RC ring oscillator can be approximated as

$$Q_{RC} \cong \frac{2}{\sqrt{k}} \qquad (\text{for } k \gg 1), \tag{1.13}$$

following from equation A.10c of the Appendix.

Using equation 1.13, the effective Q-factor for the oscillator model of Figure 1.4 is therefore approximately 0.2. This extremely low Q-factor enables a very wide locking range for the oscillator.

From the observations made above, it follows that raising the dominant pole frequency will raise both ω_o (i.e., the center of the frequency locking range), and the output amplitude. A consequence of spacing the two poles closer together is that (along with decreasing k,) the slope of the phase curve at ω_o becomes steeper and effectively decreases the locking range of the oscillator (for a given input signal amplitude).

1.3.1 Estimating the Injection Locking Range

The final step required to make this analysis complete is to verify the locking range formulas presented in this chapter to the model. Substituting either (1.12) into (A.13c) or equivalently (1.13) into (1.1) yields the necessary condition for locking as

$$\frac{E_1}{E} > \frac{4}{\sqrt{k}}\left|\frac{\Delta\omega_o}{\omega_o}\right|. \tag{1.14}$$

The only parameter outstanding now is the oscillation amplitude E. In order to further simplify calculations, the *tanh* function of equation 1.3 which describes the differential output current of the emitter-coupled transistors (Q_1 and Q_2) will be approximated by the signum function

$$I_{od} = \begin{cases} +\alpha_F \dfrac{I_{EE}}{2} & , (v_{id} > 0) \\ -\alpha_F \dfrac{I_{EE}}{2} & , (v_{id} < 0) \end{cases}. \tag{1.15}$$

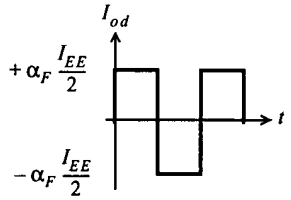


Figure 1.9 Graphical representation of equation 1.15

The fundamental frequency component of a unity square wave signal, as depicted in Figure 1.9, from Fourier analysis has an amplitude of $\frac{4}{\pi}$. Thus the fundamental frequency component of I_{od} can be approximated as

$$I_{od}' = \frac{2\alpha_F I_{EE}}{\pi}. \tag{1.16}$$

Using equation 1.16, the differential output voltage (taken as $V_I = E$) can then be expressed as a function of the injection-locked oscillation frequency, ω_i as

$$E = \frac{\left(\frac{2\alpha_F I_{EE}}{\pi}\right) \cdot 2R_L}{\sqrt{1+\left(\frac{\omega_i}{\omega_{p1}}\right)^2}} \quad (1.17)$$

In equation 1.17 we have neglected the effect of the second-pole (shown in Figure 1.4) on the oscillator's output amplitude taken at V_I. This is justifiable since the 3dB frequency of f_{p2} (9GHz) is approximately a decade beyond than the expected operating frequency of the oscillator (900MHz).

Assuming $\omega_i \gg \omega_{p1}$ and letting

$$K_o = \frac{4}{\pi}\alpha_F I_{EE} R_L, \quad (1.18)$$

results in

$$E = \frac{K_o \omega_{p1}}{\omega_i}. \quad (1.19)$$

Evaluating equation 1.19 for the oscillator's amplitude at the free-running frequency ω_0 using $\omega_{p1} = 2\pi(79.6MHz)$ results in $E = 332mVp$ which is close to the expected 340mV measured in HSPICE.

Finally, to calculate the locking range of the oscillator, equations 1.7, 1.19 and 1.10 can be substituted into equation 1.14 to obtain the lower and upper frequency locking boundaries as,

$$\omega_L = \frac{\omega_o}{1+(E_1/E_o)} \quad (1.20)$$

and

$$\omega_H = \frac{\omega_o}{1-(E_1/E_o)} \quad (1.21)$$

where,

$$E_o = \frac{4K_o}{k}. \tag{1.22}$$

The locking boundaries are defined as the frequencies beyond which the oscillator cannot remain synchronized to the injected source over an indefinite period of time. The symptoms of an unlocked oscillator near the boundary frequency are easily identified. Typically, at the threshold frequency where the oscillator cannot maintain lock, the output is severely amplitude modulated by a low beating frequency. The oscillator's output frequency in this condition appears to chirp between the injected signal's frequency and somewhere near it's free-running frequency over each beat cycle. An interesting mechanical model to help visualize the cause of this phenomenon is described in[38].

Table 1.1 Comparison of the Locking Boundaries for E_1=50mVp Injection

Calculation Method	$f_L = 2\pi\omega_L$	$f_H = 2\pi\omega_H$
HSPICE (benchmark)	670MHz (466mVp)	1270MHz (231mVp)
Simulink f_{p1}=78MHz and f_{p2}=9.0GHz	670MHz (477mVp)	1325MHz (222mVp)
Equations 1.20 and 1.21 with (1.19); f_{p1}=79.6MHz and f_{p2}= 10.13GHz	630MHz (473mVp)	1562MHz (191mVp)
Oscillator amplitude predicted by Equation 1.19 for 670 and 1270MHz.	445mVp @ 670MHz	235mVp @ 1270MHz

Table 1.1 compares the locking range and output amplitude predicted by hand analysis to HSPICE and Simulink results. The simulink upper and lower locking boundary frequencies agree well with HSPICE as do the predicted oscillator output amplitudes at those frequencies. Hand analysis using equations 1.4, 1.5, and 1.6 to calculate the pole frequencies and 1.19, 1.20, and 1.21 to calculate the boundary frequencies and respective amplitudes also agreed reasonably well to HSPICE simulations. The hand calculated solution should not be expected to agree with HSPICE as well as the Simulink model did mainly due to the approximations made in equations 1.15 and 1.16.

1.3.2 Useful applications for an Injection Locked Ring Oscillator

Typical single-phase oscillators require a resonant tank which comprises an inductor (L) and capacitor (C) network. In an integrated circuit, the realization of inductors are problematic. They are very lossy (i.e. a relatively low quality factor), have a high capacitance to the substrate of an IC thus injecting signal into the substrate and they generate large electromagnetic fields which couple undesirable spurious products to other circuit blocks by mutual coupling to other conductors including bondwires and other inductors such as those typically found in the low noise amplifier section of an integrated receiver, or in an oscillator.

One of the key advantages of the injection-locked ring oscillator technique is that many of the features and uses of an injection locked oscillator can be implemented in an integrated circuit without the need for inductors. This is because a well known feature of the ring oscillator is that it can be realized with resistive loads (identified as components R_L in Figure 1.3), thus eliminating the need for inductors. Injection locking the ring oscillator in its fundamental mode (i.e. such that its oscillation frequency of the ring is synchronized with the input source), allows all of the properties of injection locked oscillators to be realized. These properties (many of which are described mathematically or qualitatively in this paper) can then be exploited to perform many useful functions in an integrated circuit. The injection locked ring oscillator can be used as a regenerative amplifier. Using a single-phased injection locked oscillator to perform signal amplification is in the prior art[30]. There are however, no examples in the literature which illustrate the use of an injection locked ring type oscillator to perform the same function. Even more specifically, there are no examples of ring type oscillators, having a differential topology (as shown in Figure 1.3) which use resistive loads and which are locked in their fundamental mode of oscillation for the specific purpose of using any of the multiphase outputs of the oscillator to provide a useful purpose. The signals (such as V_I and V_Q for example) found within the nodes of an injection locked ring oscillator can be used to provide regenerative amplification of the injecting signal by taking said nodes as outputs.

In fact, this invention of an injection locked ring oscillator (ILRO) can be used to implement many of the useful and fundamental injection locked (single-phased) oscillator based circuits which are well known in the state of the art today. The ILRO can be used as a

signal phase shifter. The multiphase oscillator naturally has many output signal phases which will all be synchronized to the injecting signal when injection locked. These output phases of the injection locked multiphase oscillator also change with respect to the injected signal when the injected signal amplitude or frequency changes with respect to that of the ILRO. These are properties of the well known single-phase ILO which are being expanded to the concept of an ILRO. By adjusting the free running frequency of the ILRO by any of the well known means of doing so (such as adjusting the load impedances of the ring or the bias currents at the tails of the differential pair amplifiers) the locked phase of the oscillator will shift with respect to the injected signal phase, providing a means of electrically controllable phase shifting.

The topology of the ring oscillator used to implement a given injection locked oscillator function vary considerably according to the required application. Single-ended CMOS logic type inverters are known to form ring oscillators by connecting an odd number of stages in a ring. This type of oscillator can be injection locked by coupling an injected input signal to any node in the ring. An odd number of stages can be then used to generate an odd harmonic of the fundamental by coupling the various phases generated by the ring to a common node. Coupling may be done most commonly using a passive electrical element and preferably a capacitance to avoid dc bias coupling.

If the injection locked ring oscillator is of the quadrature type (i.e. usually realized using an even number of phases), then the I and Q output signals of the oscillator can be multiplied together using an analog means of multiplication (such as a gilbert multiplier) to provide a means of frequency demodulation (by low-pass filtering the output of the multiplier). This derives directly from the mathematical analysis which shows that the phase error between the I and Q outputs of the injection locked ring is proportional to the frequency error between the injected input signal and the free-running frequency of the ring. The I and Q signals are only in exact quadrature when the injected signal frequency is equal to the free-running frequency.

The ILRO can also therefore be used as an I-Q phase modulator by modulating the free-running frequency of the ring (by varying the bias or impedances in the ring) while it is in the locked condition. The I and Q phases will then shift with respect to one another, and with respect to the phase of the injected signal providing a number of phase modulated outputs.

2) Regenerative Frequency Doubling Using an Injection Locked Ring Oscillator

In this chapter, the fundamental characteristics of an injection-locked ring oscillator (ILRO) are exploited with a new ILRO based frequency-doubling technique. The basic concept is presented, followed by a mathematical analysis of the signal doubling mechanism itself. The fundamental properties and characteristics of the regenerative doubler are then discussed in the context of the ILRO core. Finally, variations of the basic regenerative doubler are presented which offer some interesting system design options.

2.1 Concept Introduction

LO signal frequency doubling can provide a number of options for generating the LO signals required in a receiver yet only a handful of IC-compatible frequency doubling methods are found in the literature [23,24,25,26,28]. In general, most doubling techniques are limited by either having a single-ended or unbalanced output, or they require filtering between cascaded stages due to the undesired harmonic content present in the output.

It is well known that an injection-locked oscillator, when employed as a constant envelope RF amplifier, can have an extremely high power-added efficiency over it's injection locking range[30]. This characteristic of an injection-locked oscillator also applies to injection locked ring oscillators (ILROs). By using an ILRO technique to perform frequency doubling, this advantage of high power-added efficiency is exploited in this technique.

Traditional methods of regenerative frequency multiplication are generally based on the concept of sub-harmonic injection-locking[31]. In such a technique, an LC-tank based (single-phase) oscillator is locked to an input frequency source set to an integer sub-multiple of the oscillator's fundamental frequency. The non-linear characteristics of the oscillator's devices are relied upon to multiply the frequency of the input signal (*fin*) up to higher integer harmonics (e.g. 2*fin*, 3*fin*, 4*fin*,... n*fin*). If one of these harmonics falls within the locking

range of the oscillator, then the oscillator will become locked to that harmonic and essentially will act as a selective harmonic amplifier. Although this technique works well, the stray coupling effects and area penalty of the inductor required for the oscillator core can be very undesirable. Especially in an IC design where other sensitive inductors are required (e.g. LNA input matching stage).

Injection-locked ring oscillators, in general, have a number of fundamental properties which make them suitable for LO signal frequency doubling in an IC. Firstly, the output signal amplitude is relatively independent of the injected signal amplitude. This is beneficial since amplitude modulated (or AM) noise is suppressed by the oscillator, and a constant output signal amplitude is obtained.

An injection-locked oscillator can also be thought of as a phase locked loop (PLL) with a wide closed loop bandwidth. The settling time of an injection locked oscillator is typically on the order of a few cycles of RF oscillation. For a 1 GHz ring oscillator, for example, this translates to a PLL with a closed loop bandwidth on the order of 300MHz.

With this concept in mind, other characteristics can be discussed. Consider the properties realized by Frequency Modulated (FM) receivers which employ phase locked loop (PLL) demodulators. Once the desired FM signal is captured (or locked), the PLL inherently minimizes the effect of noise or interference by other nearby carriers, as long as the interfering signals are weaker than the desired FM input[32]. In a similar way, the injection locked ring oscillator suppresses undesired harmonics once it is locked to a higher power input carrier. This is a very useful property of ILOs which applies to the ILRO as well.

Once frequency locked, a PLL tracks closely any input signal phase variations that are within the bandwidth of its feedback loop. This implies that the phase noise of an injection locked ring oscillator will also track the phase noise of the injecting source. This means that through proper design, most circuit techniques which exploit the properties of an ILRO will preserve the phase noise of the injecting source

Thus it is also expected that the multiplied frequency outputs of an ILO based frequency multiplier are also phase-locked to the injected LO, rejecting undesired harmonics, and at the same time, preserving the phase noise of the LO source.

The doubled-frequency output signal of the injection locked ring oscillator based frequency doubler (described next) is therefore relatively free of spurious content and does not require any subsequent filtering. As a result, many ILRO based frequency doubling stages can be cascaded to realize higher levels of multiplication without adding significant undesired spurious components. As long as the entire chain of doublers are successively locked to one another, each stage regenerates the desired LO signal. There is currently no other known means to perform such cascaded doubling in an IC without the eventual requirement for filtering stages.

2.2 A Fundamentally-Locked Regenerative Frequency Doubler

A new regenerative frequency doubling technique[11], which does not require the use of inductors, is illustrated in Figure 2.1. It is a quadrature ring oscillator which is injection locked in it's fundamental mode to the input signal frequency f_{in}. The input signal is coupled to a 2-stage differential ring oscillator through capacitors C_c, and the double-frequency output signal is extracted across the emitter-coupled nodes of differential amplifiers within the ring.

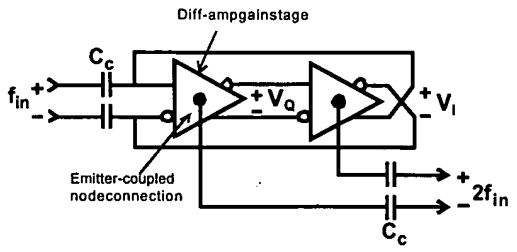


Figure 2.1 Regenerative doubler block diagram

A schematic diagram of the doubler is shown in Figure 2.2. The oscillator topology is similar to that of the circuit model used in the previous chapter (Figure 1.3) except that there are no emitter-followers between the stages; this results in less delay around the loop and allows for a higher frequency of operation.

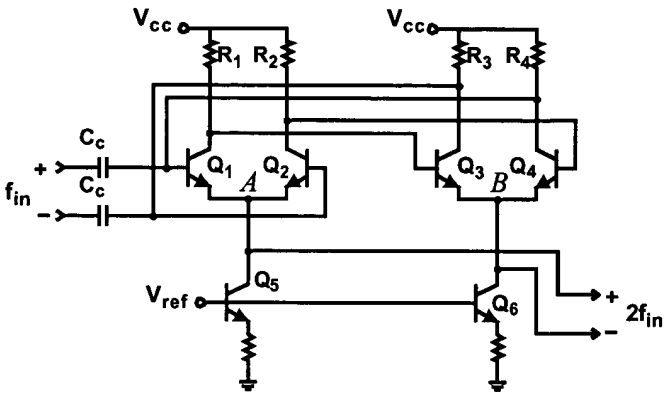


Figure 2.2 Regenerative doubler simplified schematic diagram

The doubled-frequency ($2f_{in}$) output voltage is taken differentially across the emitter-coupled nodes of the two amplifiers in the ring (marked as nodes A and B in Figure 2.2). These A and B outputs are anti-phase (0° and 180°) as a result of the 0° and 90° phased input signals appearing at the base nodes of the transistor pairs Q_1,Q_2 and Q_3,Q_4 respectively.

There are many advantages that are immediately realized with this technique: Good power efficiency (i.e. low-power ring oscillator design can be employed), high operating frequency range (output to greater than $f_T/2$), and a very wide locking range (> 50% rel. BW) is possible. Since the oscillator is being locked in it's fundamental mode of oscillation, equation 1.1 is valid. It implies that if the oscillator's output amplitude is scaled down by design, then the input signal amplitude requirement will also scale down proportionally. Another benefit of this technique is that the ring oscillator can also be designed for low or high-frequency operation without consuming significant chip area compared to other schemes which require the use of inductors.

2.2.1 Emitter-Coupled Doubling Mechanism

The frequency doubling mechanism which generates the doubled-frequency output in the oscillator is based on large-signal rectification. In small-signal analysis, the emitter-coupled

node of a transistor differential pair (Figure 2.3) is often considered an ac ground. For signals larger than approximately $2V_T$, the signal voltage at the emitter-coupled node is not zero and consists of mainly even-order harmonics due to the full-wave rectification by the base-emitter junctions of transistors Q_1 and Q_2.

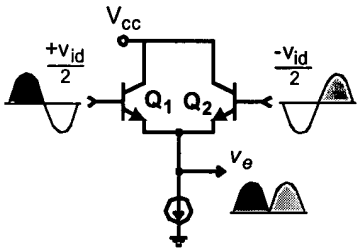


Figure 2.3 Emitter-coupled pair driven in a large-signal model

The voltage at the emitter-coupled node is determined from the large signal equation for the base-emitter junction voltage,

$$V_{BE} = V_T \ln \frac{I_C}{I_S} . \tag{2.1}$$

Using equation 2.1 and Kirchoff's voltage law to express the base-emitter junction voltages for transistors Q_1 and Q_2 of Figure 2.3, the emitter-coupled node voltage, V_E is

$$V_E = \frac{V_T}{2}\left[1 + \cosh\left(\frac{V_{ID}}{V_T}\right)\right] + (\text{dc term}) \quad . \tag{2.2}$$

Corrections for the large-signal parameters of Nortel's 0.5um x 5um, 25GHz f_T transistors results in a device-specific equation:

$$V_E = 3.2 \cdot \frac{V_T}{2}\left[1 + \cosh\left(\frac{V_{ID}}{3V_T}\right)\right] + (\text{dc term}) \quad . \tag{2.3}$$

Equation 2.3 matches the characteristic of a diff-pair simulated in HSPICE to within 2%. Both characteristics are plotted in Figure 2.4 after subtracting their respective dc bias voltages.

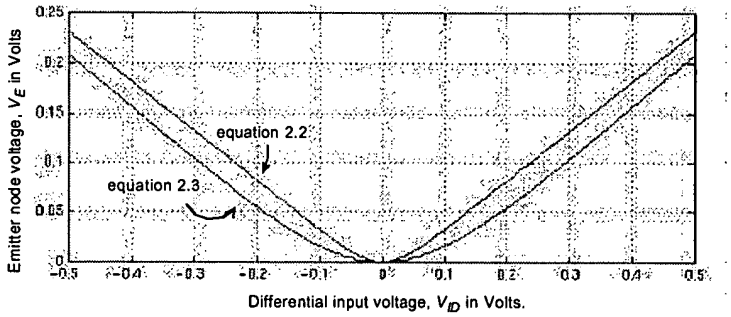


Figure 2.4 Emitter-coupled node voltage as a function of differential input voltage

For $\|V_{ID}\| \sim > 2V_T$, the equations plotted above are similar that of a full-wave voltage rectifier $V_e = \frac{1}{2}\|V_{ID}\|$, except for the dc bias shift.

A similar characteristic is also found at the source-coupled node of a CMOS differential pair. All of the techniques illustrated in this thesis using bipolar devices could also be realized using CMOS devices, with only minor modifications.

Figure 2.5 is obtained through fast-fourier transform (FFT) analysis of V_E from equation 2.3 for a single-tone sinusoidal input signal. The amplitude of the second harmonic ($2f_{in}$) component as a function of input signal amplitude and as a fraction of the input signal amplitude (or voltage conversion efficiency $\|V_{2nd}\|/\|V_{fund}\|$) is plotted. It should be noted that there is current gain, although the voltage gain is less than unity. For each half-cycle of input, one transistor drives the emitter load as an emitter-follower, while the other transistor is essentially turned-off. This provides a low output impedance and good signal driving capability at very high frequencies (to $f_T/2$) compared to circuits which have an output connected to the collector of the transistor.

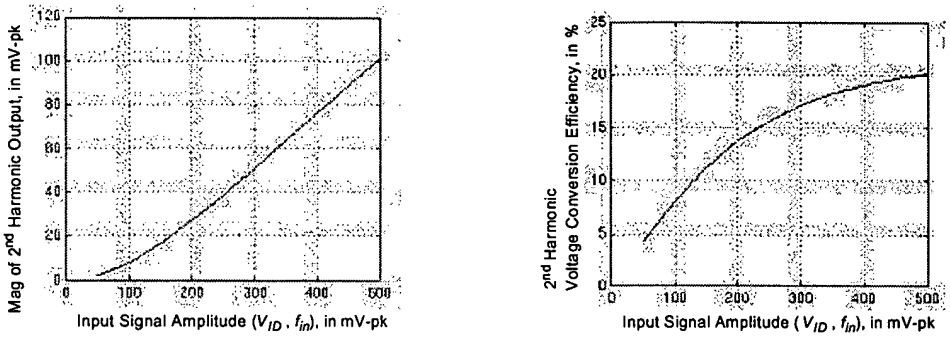


Figure 2.5 Voltage Conversion

An important quality of a frequency doubling circuit is its ability to suppress feed-through or 'leakage' of the input fundamental harmonic to the output. In the circuit of Figure 2.3, the fundamental-frequency input will only be suppressed from appearing at the output node (V_E) if the transistors are well matched, have an identical dc bias, and are driven from a purely differential input source. Any common-mode component at the input couples directly to the emitter-coupled output. Since transistor matching and dc bias can be controlled well in an IC, the suppression of the fundamental signal at the output depends almost entirely on accurate balance of the differential input signal.

In the regenerative doubler (Figure 2.2), capacitive coupling of the input signal to the oscillator allows the oscillator to maintain a balanced dc bias point through symmetry, even while oscillating. Ideally, the dc component in each of the base node voltages of Q_1-Q_4 should be identical. The differential structure of the oscillator and the oscillator's strong feedback also work to keep the input signals to the transistor pairs in a differential mode. Even if the input source is entirely single ended, the oscillator's strong feedback causes the input transistor pair to see a differential-mode signal across it's base nodes.. These properties of the differential ring oscillator topology work to suppress the fundamental component from appearing at the emitter-coupled output nodes.

2.2.2 I-Q Phase Errors in the Ring due to Injection

A resistively-loaded ring oscillator typically has a low Q-factor and therefore requires a relatively small amount of phase shift in the feedback loop to alter the free-running frequency.

When the ring oscillator is locked at a frequency other than ω_o, the V_I and V_Q outputs of the ring (see Figure 2.1) have a small phase error, φ_ε from 90° or quadrature caused by the injected signal. The magnitude of this phase error depends on how far the locked oscillator frequency is from the natural free-running frequency and the oscillator's Q.

Using equation 1.1, an oscillator with a Q-factor of 0.2 (such as that of Figure 1.4), and a 50% relative locking range will have a quadrature phase error (φ_ε) of approximately 0.2 radians or 11° at the band edges. Across the emitter-coupled output nodes of the oscillator (*A* and *B*), this translates to a 22° phase error (or $2\varphi_\varepsilon$)from the ideal anti-phase (180°) condition due to equation 2.1. This non-fully-differential output signal can be represented by the sum of a fully-differential signal and common-mode signal. If φ_ε is zero, then the output signal is fully differential. If φ_ε is 90°, the signals at *A* and *B* will be in phase, and the output signal is therefore entirely a common-mode signal. For an ac signal amplitude of *Ao* at each of the nodes *A* and *B*,

$$Av_{diff} = 2A_o\cos(\varphi_\varepsilon) \tag{2.4}$$

$$Av_{comm} = A_o\sin(\varphi_\varepsilon), \tag{2.5}$$

leading to the suppression of the common-mode expressed in dB with respect to the fundamental as

$$\text{Common-mode suppression} = \frac{V_{diff}}{V_{comm}} = 20\log(2\cot(\varphi_\varepsilon)) \tag{2.6}$$

Consider again, the (realistic) case of an oscillator having a Q of 0.2 and an injection locking range of 50%; an extreme locking range for most applications. With $\varphi_\varepsilon = 11^o$, equation 2.6 describes the common-mode signal as being suppressed below the differential signal by > 20dB.

Subsequent differential RF stages, such as a buffer or a mixer typically provide further common-mode rejection such that the common-mode signal can be considered relatively

small for most practical purposes. It is therefore suggested, that the differential output can be considered almost fully-differential for most practical design purposes.

It was determined in the previous chapter that the output amplitude of the oscillator of Figure 1.4 is approximately 340mV-peak. Using the characteristic of Figure 2.5, the doubled-frequency output at the emitter-coupled nodes is expected to be approximately 62mV-peak (in 0^o and 180^o phases). When this output is taken differentially across the two emitter-coupled nodes, it is ~ 124mV-peak.

2.3 Regenerative Doubler Variations

There are many variations of the basic doubler which can provide unique options to the designer. A few of the more interesting concepts are presented briefly below.

2.3.1 Regenerative Frequency Quadrupler

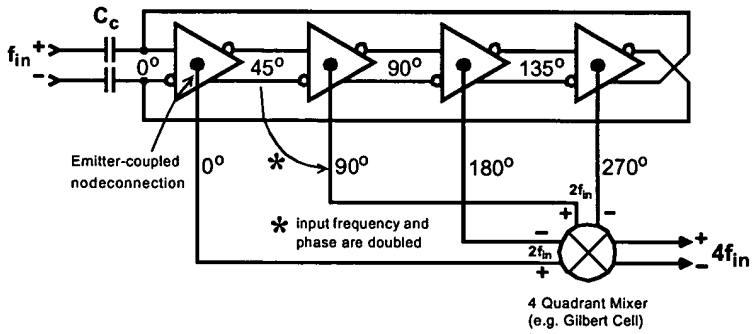


Figure 2.6 Regenerative Frequency Quadrupler

In this realization, the 4-stage ring naturally generates 4 unique fundamental frequency phases (labeled 0^o, 45^o, 90^o, and 135^o). The four double-frequency emitter-coupled node signals form two fully-differential signal pairs that are 90^o phase shifted. These double-frequency quadrature signals can then be multiplied together using a 4-quadrant analog multiplier, such as a Gilbert multiplier, to generate a fully-differential $4f_{in}$ output signal.

2.3.2 Regenerative Frequency Tripler

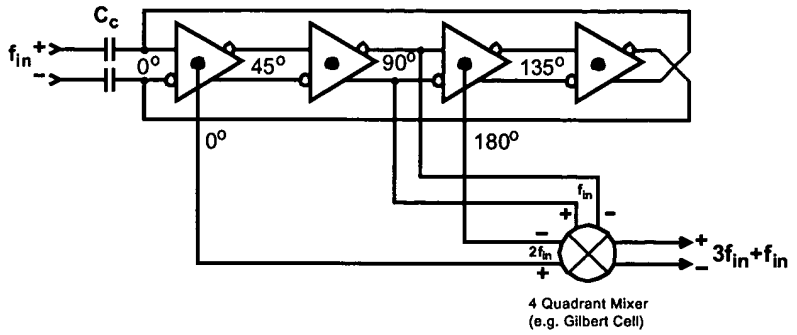


Figure 2.7 Regenerative Frequency Tripler

The circuit of Figure 2.7 provides a frequency tripling function by multiplying the fundamental signal circulating around the ring with one of the double frequency signals. The result is a $3f_{in}$ signal summed with an f_{in} signal.

2.3.3 Frequency Tracking ILRO

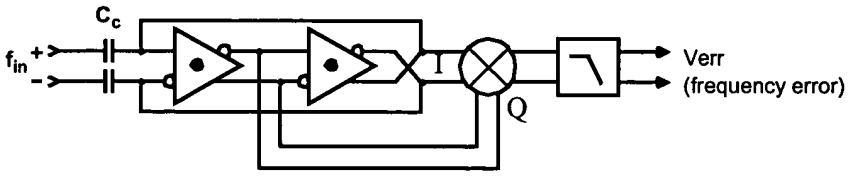


Figure 2.8 A Frequency Tracking Injection Locked Ring Oscillator

An interesting property of the injection locked quadrature oscillator is that the I and Q outputs are only in exact quadrature when the oscillator is locked at its free-running frequency. This property could be exploited to calibrate the oscillator's center frequency, or to provide frequency tracking capability.

In Figure 2.8, the I and Q outputs of the ring are multiplied together using a 4-quadrant multiplier and then passed through a low pass filter.

$$\cos(\omega t)\cdot\cos\left(\omega t+\frac{\pi}{2}+\varphi_\varepsilon\right)=\frac{1}{2}\left[\sin(\varphi_\varepsilon)+\cos\left(2\omega t+\frac{\pi}{2}+\varphi_\varepsilon\right)\right] \quad (2.7)$$

Low pass filtered

$$v_{err}=\frac{1}{2}\sin(\varphi_\varepsilon) \quad (2.8)$$

The resultant error signal v_{err} is a d.c. voltage defined by equation 2.8. This signal can be used to indicate the error between the free-running frequency of the oscillator and the frequency to which it is currently locked. If the ring oscillator were redesigned as a V.C.O., a negative feedback loop could allow v_{err} to control the free-running frequency of the oscillator and cause it to track the injected signal. This would essentially cause the I and Q outputs to remain in precise quadrature for all locked frequencies. Since the frequency error v_{err} is proportional to the input frequency, it can be directly used for frequency detection, relative frequency difference measurement, or for frequency demodulation purposes.

3) A Frequency Halver (or divide-by-2) with Precision Phase Tuning

In the last chapter, a new method for ILRO based regenerative frequency doubling was presented. In this chapter, the motivation for a quadrature LO signal generator having a phase tuning input is provided in the context of an image reject mixer. The concept of a regenerative frequency halver is then presented with the aid of another Simulink model, similar to that which was used to describe ILRO behaviour. From this model, a new technique for providing a precision phase tuning capability is suggested along with a practical method for realizing the desired phase tuning functionality.

3.1 A Regenerative Frequency Halver (Divider)

Frequency divide-by-2 circuits which are based on analog injection locking techniques to perform the frequency division are known as frequency halvers or regenerative dividers.

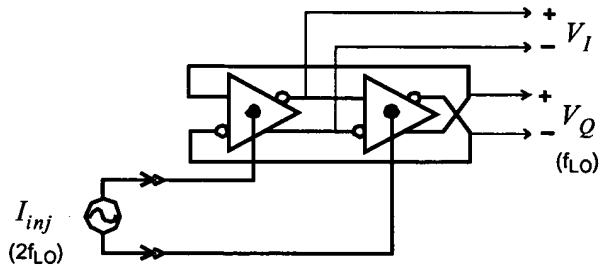


Figure 3.1 Frequency halver block diagram

Shown in Figure 3.1 is a block diagram of a frequency halving circuit which was first presented in [18] using the circuit topology of Figure 1.3 to realize the differential amplifying stages of the ring. Referring to Figure 3.1, a differential ac current source is connected across the emitter-coupled nodes of the ring and is set at a frequency which is twice that of the

fundamental frequency of the ring. This causes the doubled-frequency emitter-coupled node voltages of the ring oscillator to become synchronized to the injected currents of I_{inj}. This topology is very similar to the regenerative frequency doubler in Figure 2.1 except that the input and output ports are reversed. An important feature of the halver is that emitter-coupled $2f_{LO}$ input signal injection is symmetric with respect to the topology of the ring since the injected currents affect both amplifying stages of the oscillator identically. The result of this symmetry is that the outputs V_I and V_Q remain in precise phase quadrature for the entire locking range of the oscillator, not just at the center (or free-running) frequency of the oscillator. The frequency of the quadrature outputs are half that of the injected current and so the circuit performs a frequency divide-by-2 (or halving) function.

3.2 Simulink Model of the Regenerative Frequency divider

A Simulink model can be used to predict the behaviour of the regenerative divider. Using the circuit shown in Figure 1.3b to realize the differential amplifiers of the oscillator in Figure 3.1, the Simulink model (shown in Figure 3.2) is obtained.

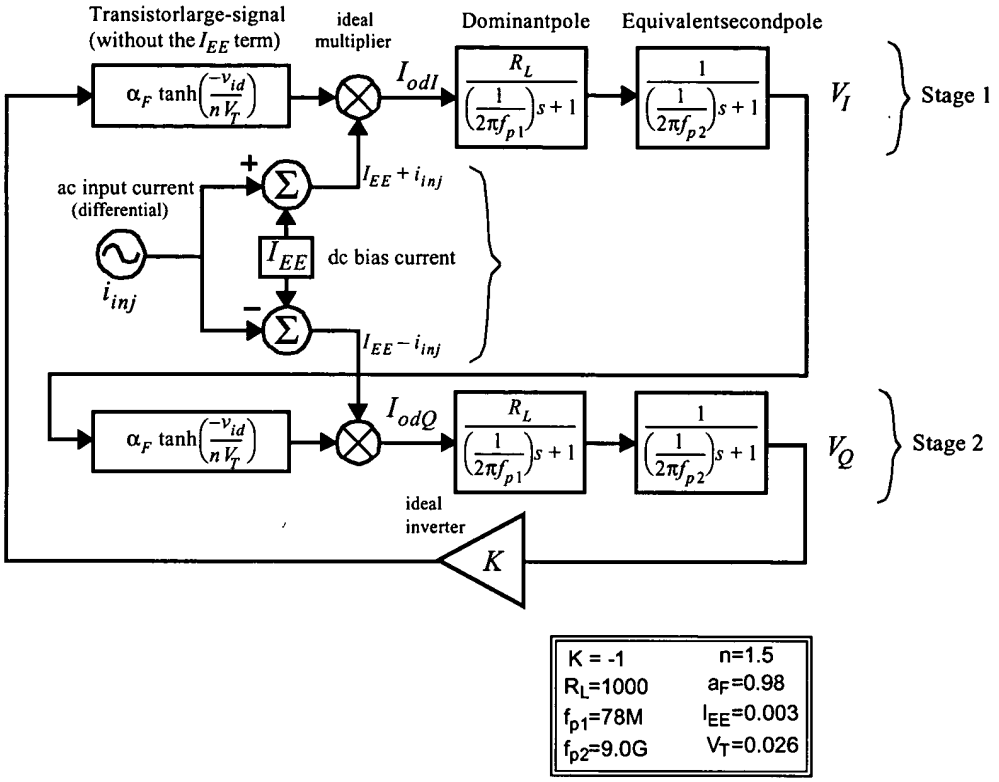


Figure 3.2 Simulink model of the regenerative divider in Figure 3.1

I_{EE} is the dc bias current for the emitter-coupled pair Q_1-Q_2 in Figure 1.3b, and is assumed to be much greater than the amplitude of the differential input RF current I_{inj} (i.e. $I_{EE} \gg \|I_{inj}\|$). The input signal I_{inj} is an ac differential current source and therefore adds with 0° phase to the I_{EE} bias current for one of the stages and with 180° phase to the I_{EE} bias current for the other stage. The result is a pair of differentially-modulating bias currents which are then multiplied by the respective *tanh* functions of each diff-pair to obtain the differential large-signal transistor output currents I_{odI} and I_{odQ} in the model. The parameters of the oscillator in this model are identical to the model described in Figure 1.4 since the same circuit is being used for the gain stages (Figure 1.3b).

With an input signal amplitude of 310uA-peak, HSPICE simulations predict that the oscillator will have a lower frequency locking boundary of 1.38GHz (injected frequency)

which compares favourably to the 1.40GHz prediction from the Simulink model. Simulink also predicts that the upper locking frequency boundary is 2.30GHz whereas HSPICE predicts 2.20GHz. The error of this Simulink model at the higher frequency end of the range is likely due to higher order poles in the real circuit that are not accounted for in the model (e.g. Cμ, Rb, etc.)

The model of Figure 3.2 also implies that the quadrature output amplitudes of the frequency halver are defined by Equation 1.19 with a -6dB/octave response, where ω_i is equal to the output frequency of the halver.

3.3 Precise Phase Control of Quadrature LO Signals

As was mentioned earlier, the I and Q output phases of the regenerative divider remain in precise quadrature throughout the locking range of the oscillator. In practice, this can be achieved with a phase error on the order of $< 1^{\circ}$.

In the realization of Figure 3.3, emitter-followers are not used between amplifying stages to allow for a lower supply voltage and an increased maximum operating frequency range. The injected double-frequency signal ($2f_{LO}$) is capacitively coupled to the emitter-coupled nodes to illustrate a practical means of injection.

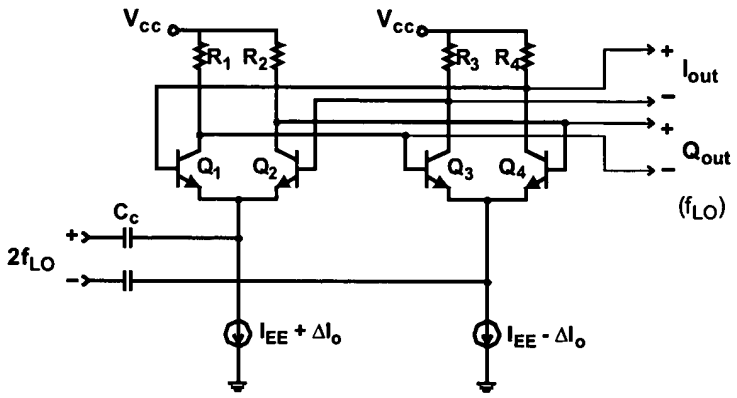


Figure 3.3 Regenerative Divider Simplified Schematic Diagram

Normally, the time delays through each stage of the ring oscillator are well-matched due to the electrical symmetry of the two stages of the quadrature ring. By intentionally disrupting the symmetry of the ring, the time delay (or phase) through each stage of the ring is altered, resulting in a slight phase shift between the I and Q outputs away from quadrature.

From a frequency-domain perspective, the frequencies of the higher order poles of each diff-pair are sensitive to the transistor's bias current. By differentially altering the bias current through each stage in the ring, the higher-order poles of each amplifier will shift in opposite directions, thus, intentionally altering the phase relationship between the quadrature outputs of the ring. Figure 3.3 illustrates a small offset current (ΔI_o) being added differentially to the bias currents I_{EE} to perform the phase shift.

There are two important features of this new phase tuning technique: firstly, since the control mechanism for phase shifting is through a dc bias offset, it is relatively easy to make very small phase changes (on the order of $< 0.1^{\circ}$) between the quadrature outputs of the ring. The smaller the dc offset, the smaller the phase change. secondly, unlike the frequency-dependent phase shift found in an RC-network for example, the induced phase shift in the oscillator is strongly independent of the frequency of oscillation. This is because the phase shift is a result of the difference between two frequency-dependent time delays in the ring.

This implies that if a given phase shift is intentionally calibrated at one frequency, it will not need to be re-calibrated at other nearby frequencies.

3.4 A method to allow radio transceivers to perform self calibration of image-reject-mixers.

The purpose of this section is to describe a method for the realization of a self calibrating image-reject mixer architecture within a radio transceiver. This method provides a practical means for allowing a portable wireless device (such as a cellular telephone) to calibrate its internal receive and transmit image-reject-mixer's phase and amplitude errors without the use of an externally applied test signal. Specifically, the transmitting circuitry (or sub-blocks) of a transceiver can be used to generate the test signals required to calibrate the image-reject-mixers in the receiver sections (or circuit-blocks), and the receiver sections can be used to calibrate the image-reject-mixers of the transmitter.

First some important concepts are briefly discussed.

3.5 Conventional Heterodyne Front-End Topology

Shown in Figure 3.4 is a conventional front-end topology commonly used in high-performance receiver front-ends. Both the desired RF band and an unwanted image band are converted to the same IF since they share the same frequency separation from the LO carrier. In this topology, discrete filters are used to suppress the image band. A total image rejection (IR) on the order of 70-100dB is typically required[36]. The preselect filter band-limits the input to prevent out-of-band carriers from desensitizing or overloading the LNA. The preselect filter also provides some IR, typically on the order of 30dB, if the image band is outside the passband of the filter. The rest of the image rejection is obtained by a second off-chip filter placed between the LNA and mixer. This filter is typically more aggressive than the preselect filter (~ 45dB IR,) and has a higher insertion loss (~ 3-4dB). Placing it after the LNA reduces the effect of insertion loss on the noise figure of the receiver.

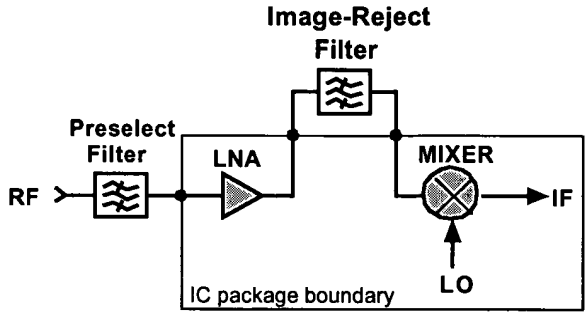


Figure 3.4 Conventional Heterodyne Receiver Front End

This topology works well for many low-cost implementations, however in an integrated receiver IC application, performance is compromised by having to route the RF signal through an off-chip filter. Wideband 50Ω matching networks are required at the RF interfaces to an IC, where the signal to be filtered then suffers board, package, and filter losses before returning back on-chip to drive the mixer. Multi-chip modules with controlled impedance packages reduce parasitics and losses but not power consumption and add significant cost. Furthermore, fixed-frequency discrete RF filters limit system flexibility in an open standard environment.

3.6 Image Reject Mixing

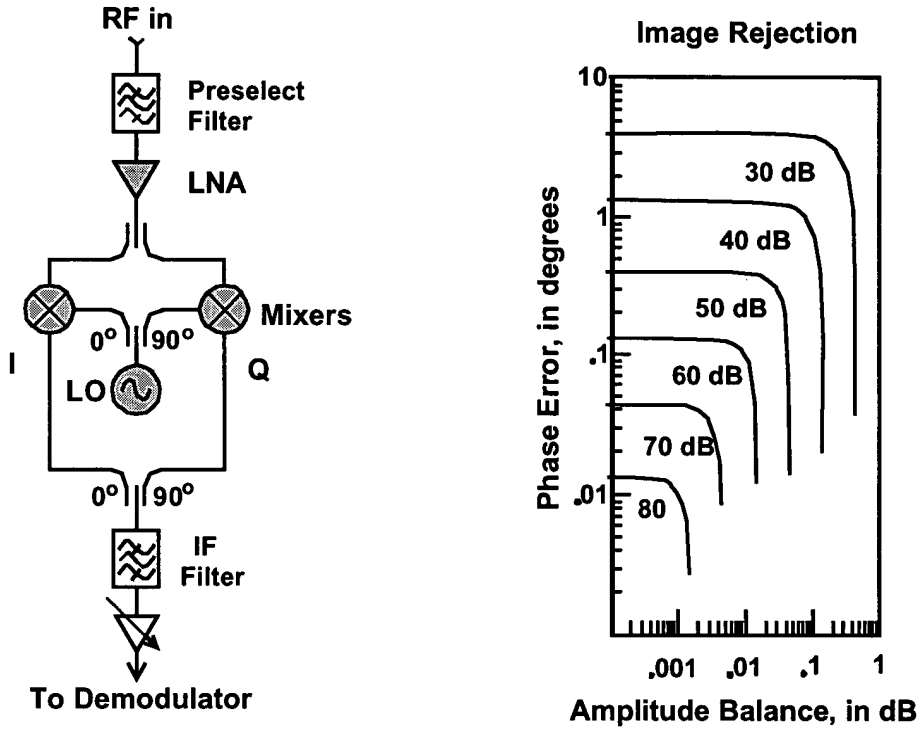
An alternative method of rejecting the undesired image carrier at IF is by using an image reject mixer architecture (illustrated in Figure 3.5a and clarified in references [14,15]). The RF input is split into two paths and downconverted by a quadrature pair of LO signals into an IF_I and an IF_Q path. The two IF paths are then phase shifted by 90° with respect to one another and then summed together, or subtracted from one another, thus yielding the desired frequency translation (i.e. above or below the LO carrier respectively).

In practice, the second 90° phase shift required at IF is one of the more difficult function to realize passively in this system. A well known active method of implementing this second shift is to use a second (quadrature) intermediate-frequency conversion (as is used in the classic Weaver architecture[15]).

It is very advantageous to perform this function in the analog domain so that any large interferers in the image band can be cancelled out prior to digitalization, where spurious components can be generated at the IF. This significantly eases the linearity requirements for the A/D.

It is well known in the art that an offset error in any of 90° phase shifts, or an imbalance in the phase or amplitude symmetry of the I and Q paths degrades the overall image rejection. One option is to cancel out any error by providing an equal and opposite phase shift in the quadrature LO phases. Amplitude offset errors in the I and Q paths through the image-reject architecture can also be tuned-out by applying a correcting gain factor. The problem is determining the proper amplitude and phase corrections required.

Figure 3.5b shows a plot of the image rejection calculated as a function of the total phase and amplitude error in an image-reject-mixer. The quadrature LO accuracy attained using most high-frequency I-Q signal generation techniques is on the order of $< 1^{o}$ resulting in a maximum image rejection on the order of ~ 40-50 dB. This assumes that an ideal IF quadrature combiner is available and that no quadrature LO phase tuning is performed.



a) Hartley receiver downconverter

b) image rejection vs. amplitude and phase errors in quadrature signals

Figure 3.5 Image reject mixer topology and rejection

The frequency halving circuit (I-Q generator) illustrated in Figure 3.3, is one means of fine adjusting the quadrature LO phases. This phase tuning ability enables the systematic offset in an image-reject-mixer to be removed, thereby maximizing image-rejection of the receiver.

One way to correct the phase and amplitude errors in an image-reject mixer is to apply a test signal in the image band of the image-reject mixer and then to adjust the image-reject mixer's internal parameters (such as gain and phase) with the goal of maximizing the image-rejection attained.

There are many different implementations of the image-reject mixer and many different ways to calibrate such receiver architectures but most methods have a common requirement. A test carrier is required to be present within the receive band of the transceiver for the

purpose of detecting and eliminating the unwanted image signal through image-reject mixer calibration.

It is proposed here that a test carrier can be generated by the transmitter section of a transceiver and can be internally coupled to the receiver section of the same radio transceiver for the purpose of calibrating the image-reject mixer section of the receiver or an image-reject mixer section of the transmitter. A received signal strength indicator circuit (which is found in most modern receiver systems) can be used to detect and measure the magnitude of the undesired image signal present at the output of the image-reject mixer. This information can then be used to provide the feedback information required for the calibration of the image-reject mixer. The goal of the calibration i to maximize rejection of the image carrier by compensating for phase and amplitude errors in the I and Q image reject mixer paths either in the RF (input radio-frequency), LO (local oscillator), or IF (intermediate frequency) paths. This includes in a digital domain if a digital IF section is used which has as inputs the I and Q IF signals from the front-end of the image-reject mixer architecture.

There are currently no examples in the literature of a radio transceiver which intentionally tunes the output frequency of its own transmit section to generate a test signal in the image-band of the receiver for the purpose of calibrating the image-reject mixer of the receiver. In addition, there are no examples in the literature where a radio transceiver uses it's receiver to detect the signal strength of the unwanted image carrier generated by the transmitter section for the purposes of calibrating out the phase and amplitude errors in the transmitter's image-reject mixer. The goal in this case is to reduce image-signal generation of the transmit section. Thus the image-reject mixer to be calibrated can lie in either the receive section, the transmitter section or there can be an image-reject mixer in both sections to be calibrated.

In the case of a receiver's image-reject mixer calibration where a test signal is required to be generated within the image-band of the receiver (ideally at an offset from the first LO equal to the IF output of the image-reject mixer), the test source needs to be generated at a fixed frequency. This is why the transmit section can be an effective source for this signal since in most high performance radios, the transmit section is required to be capable of synthesizing a precision frequency output in normal operation.

An alternative source for a precision frequency test signal is from the reference oscillator source used in the frequency synthesizer of a transceiver, or from the precision clock signal used to synchronize the digital logic or data circuitry of a transceiver. Both of these high precision sources are very often found in the tens of MHz region, typically far below the required frequency of the test image signal (which can be in the GHz range or on the order of a decade higher). This is not a problem since the waveform of the digital clocking or reference source can be altered from that of a pure sine-wave by clipping or limiting the amplitude of the signal. Anyone in the state of the art will immediately realize that this will give rise to higher order harmonics found at integer multiples of the fundamental frequency of the signal. The low levels of these high harmonics is actually a desirable feature due to the high sensitivity of the low noise amplifier which usually precedes the image-reject mixer in a receiver architecture. The synthesizer frequency of the first LO of the receiver can then be selected such that one of the harmonics of the clock or reference falls at the image frequency of the receiver while no harmonic falls at the desired RF input frequency of the receiver. The harmonic found at the image will then (by proper selection of LO frequency) get converted to the IF as a useful test carrier to calibrate the image rejection of the receiver.

A key feature for this system is that the transmitter circuit or test signal generating source is isolated from the antenna of the transceiver such that the test signal is prevented from radiating to the outside world during this calibration. This can be done by any means of breaking the RF path from the transmitter to the external radiating antenna, or by shunting that path to a ground potential. The RF path from the external antenna to the receiver is also broken (or shunted to ground) so that the receiver does not pick up external radio signals from it's antenna during the calibration.

3.7 A Tau-Dither Based Analog Method of Phase and Amplitude Error Offset Correction in an Image-Reject Mixer.

There are many types of error minimization algorithms (both analog and digitally based schemes) which can be used to correct the phase and amplitude of the fixed offset errors of an image-reject mixer. A manual form of an algorithm would be to inject a test signal at the

image frequency of the receiver and to observe the signal amplitude of the image in the IF output. The phase angle between the I and Q LO signals is then adjusted for maximum image rejection (or minimum IF signal magnitude). Next the gain between the I and Q paths of the image-reject mixer are tuned to find a new maximum image rejection. Ideally there should be no need to go back and readjust the phase angle, but in a practical system, phase and gain controls are not quite independent. With a few iterations back and forth between adjusting phase and then the gain, the performance of the image-reject mixer can be drastically improved.

An analog technique which is well suited to correct the phase and gain offset errors in a transceiver application, is based on the Tau-Dither minimization technique[37].

Shown in Figure 3.6 is a typical curve of the test image signal amplitude as a function of phase correction or amplitude correction control signals. It can be seen that in the portion of the curve marked as section 2, the image-signal amplitude reaches a minimum value. Note that the minimum value of image signal amplitude at IF corresponds to a maximum image rejection goal for the calibration.

Assume for the moment that a phase offset error in the image-reject mixer will be calibrated out first. A test carrier is input to the image-reject mixer at the image frequency of the receiver. Suppose the image signal amplitude at the IF output of the image-reject mixer is found to be at the point marked as "a" in section 1 of the curve in Figure 3.6. By increasing and decreasing (or dithering) the phase tuning control signal between points a and b, the image signal amplitude increases and decreases in a way which indicates the correct direction of optimization. In section 2 of the curve, dithering the control value between points a and b does not give rise to any directional indication and thus the control signal is at the optimum value for minimized image signal.

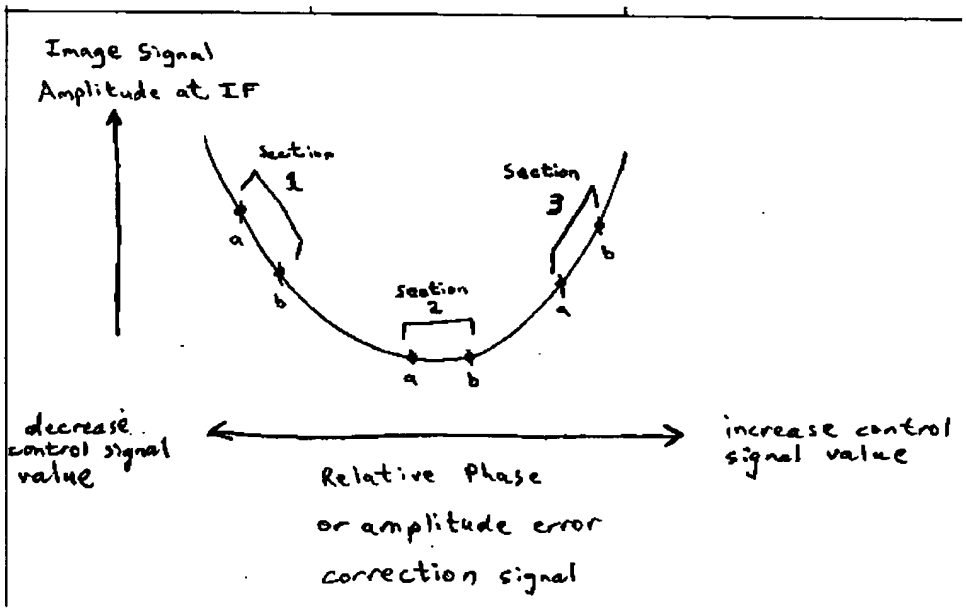


Figure 3.6 Typical Image Amplitude at IF vs. Phase or Amplitude Tuning Control Input

A preferred embodiment of a calibration loop employing Tau-Dither tracking to calibrate out the phase and amplitude offset errors in an image reject mixer is shown in Figure 3.7. Many of the annotated nodes of Figure 3.7 are plotted in Figure 3.8 as a function of the waveform of interest, the section of the curve of Figure 3.6 within which the operation is described, and as a function of time (along the x-axis of each sub-plot in the figure).

The image-reject (IR) mixer block 300 is an image-reject receiver architecture (commonly a Hartley or Weaver topology), and may be implemented using analog or digital circuit techniques or a combination of both. Upon beginning calibration, the system controller (308) will first isolate the transceiver's antenna port from the RF input port of IR mixer block 300 and from the test signal generator block 312 through an antenna isolation circuit function (312). The purpose of function 312 is to prevent external RF signals from coupling to the input (RF in) of the IR mixer during calibration, and to prevent unintentional radiation of the signal from the test signal generator block 311 out through the antenna. The test signal generator block is designed to be able to generate a signal frequency precisely at the image frequency of the IR mixer. The controller (308) can adjust the IR mixer's receive frequency through a control input to 308, and the controller may also have the flexibility of

controlling the transmitting frequency of the test signal generator (311). In one embodiment, the transmitter or upconverter of a transceiver is used to perform the required functions of block 311. Once the test signal frequency and the IR mixer's receive frequency are selected such that the test signal frequency falls at the image frequency of the IR mixer (300), the unwanted image carrier will be present at the IF (intermediate frequency) output of block 300. To begin correcting the phase errors in the IR mixer, controller 308 instructs the track and hold function (309) to go into track mode and pass the calibration control voltage directly through to the I-Q phase angle control input. Low frequency oscillator (304) is designed to generate a low frequency dither signal (see V_{LFO} in Figure 3.8) which is summed through block 307, directly to the "calibration control voltage" node and hence into the I-Q phase angle control node during phase calibration. This low frequency signal acts to dither the phase control between two nearby values (marked as "a" and "b" in Figure 3.6).

Figure 3.6 illustrates three key sections on the image signal amplitude versus control value curve. Calibration will typically begin with the calibration control voltage at a non-optimum value (either too high or too low). If at the beginning of calibration the phase error lies in section 1 of the curve, the waveforms under the heading "Section 1" in Figure 3.8 describe the signal waveforms within the calibration loop. Beginning with the output of block 304 (the LFO), the V_{LFO} timing diagram in row 'iv' shows that block 304 generates a square wave type signal. Due to the negative sign in the summation function 307, a negative (starting) value for V_{LFO} results in an increase in the calibration control voltage to the point "b" in section 1 of Figure 3.6. Half a V_{LFO} period later, the control voltage is decreased a step to point "a" in Section 1 of Figure 3.6. At point "b", the amplitude of the test carrier which appears at the IF output of block 300 is smaller than at point "a". Since the period of the V_{LFO} is by design much larger than the IF period, only the envelope of the IF signal can be observed in the V_{IF} timing diagram (row "i") of Figure 3.8. The amplitude of the IF signal can be clearly seen to follow the polarity of the V_{LFO} signal as expected in Section 1 of Figure 3.6. Note that the markings of "a" and "b" on the V_{LFO} timing diagrams of Figure 3.8 do not represent the V_{LFO} voltage value but are simply markers to identify the corresponding position on Figure 3.6 for a given value of V_{LFO}.

The purpose of circuit block 301 is to extract the amplitude (or envelope) information from the IF carrier (V_{IF}). This can be done using a simple envelope detection circuit, or an AM demodulator, or the Received Signal Strength Indicator (RSSI) of a receiver which is designed to accurately measure signal power at the IF. The timing diagram labeled V_{ENV} (row "ii" in Figure 3.8), shows the required output signal from block 301. Block 302 is then employed to remove the dc content from this signal V_{ENV} and any other frequency content which is not near the frequency of the LFO (block 304). The timing diagram V_{AM} in Figure 3.8 illustrates the output from block 302 if it is realized using a band pass filter designed to pass only the fundamental harmonic of the LFO frequency.

The V_{AM} signal is then multiplied with the V_{LFO} using an analog multiplier (block 303) to generate signal V_M. Figure 3.8 clearly shows that the V_M signal will have a positive dc component. This dc component is extracted through the use of block 305 (which can be implemented with a low pass filter). This dc signal V_E, is a negative feedback error signal which is proportional to the negative of the slope of the curve of Figure 3.6. Notice a positive value of V_E is observed in timing diagram row "vi" in the column of "Section 1" in Figure 3.8. The polarity of the signal indicates the correct direction in which the average Calibration Control Voltage should move in order to minimize the image signal amplitude in the IF and thus improve the image rejection of the IR mixer block 300. Block 306 integrates signal V_E and adds it to the Calibration Control Voltage node to close the feedback loop of the calibration circuit. The integrator will integrate the positive value of V_E and slowly increase the calibration voltage while the incremental dithering by the V_{LFO} continues. The timing diagrams in Figure 3.8 clearly illustrate how in "Section 3" of the curve of Figure 3.6 the polarity of V_E will result in a negative value. In this case, the integrator will then correctly decrease the average value of the calibration control voltage and head towards Section 2 of Figure 3.6. At the minimum point in the IF image amplitude versus control signal curve (i.e. Section 2 in Figure 3.6), V_E is shown to be zero and therefore the calibration control voltage is at the optimum value for maximum image rejection. Once controller 308 decides to end calibration, the calibration control voltage which (during this hypothetical phase calibration) was being passed through or tracked by block 309 is then held by block 309 through a

functional control command from the controller. In this way, the calibrated value is stored and kept as input to the IR mixer block so that the mixer block retains a superior image-rejection performance achieved through the phase calibration.

With the phase calibration complete, the controller can then place block 310 in track mode and thus calibrate the gain balance of the IR mixer block. With a few iterations between gain calibration and phase calibration, a final maximum-image rejection performance will be obtained using this technique.

Once both gain and phase calibrations are finally complete, both blocks 309 and 310 are kept in hold mode for the duration of required operation of the IR mixer (block 300). Test signal generator (block 311) is no longer required and can be disengaged. The antenna can now be re-coupled to the RF input port of the IR mixer in order to use the IR mixer as a receiver for receiving radio signals through the antenna.

Anyone in the state of the art can realize how a similar feedback loop can be used to calibrate the image-rejection of the transmit section of a transceiver. The antenna is once again isolated from the transceiver to prevent unintentional signal reception or transmission and the IR mixer of the receiver (300) is set to receive (in it's non-image band), the image carrier of the transmit IR upconverting mixer (not illustrated but can be considered as similar to 300). The frequencies for the transmitter and receiver during calibration are chosen such that only the image carrier of the transmitter will fall in the IF of the receiver and thus be demodulated by block 301 of the receiver section. The calibration loop then works exactly the same way except that the calibration control voltage is also connected to other track and hold blocks which feed the phase control and gain balance control adjustment inputs to the transmitter's up converting IR mixer (not illustrated in Figure 3.7).

Calibration proceeds in the same way as described before so that the phase and gain tuning correction voltages can be stored in the transmitter's IR mixer's equivalent track and hold blocks. Once both the transmitter and receiver have been calibrated, then the antenna isolation is removed and normal radio operation may begin.

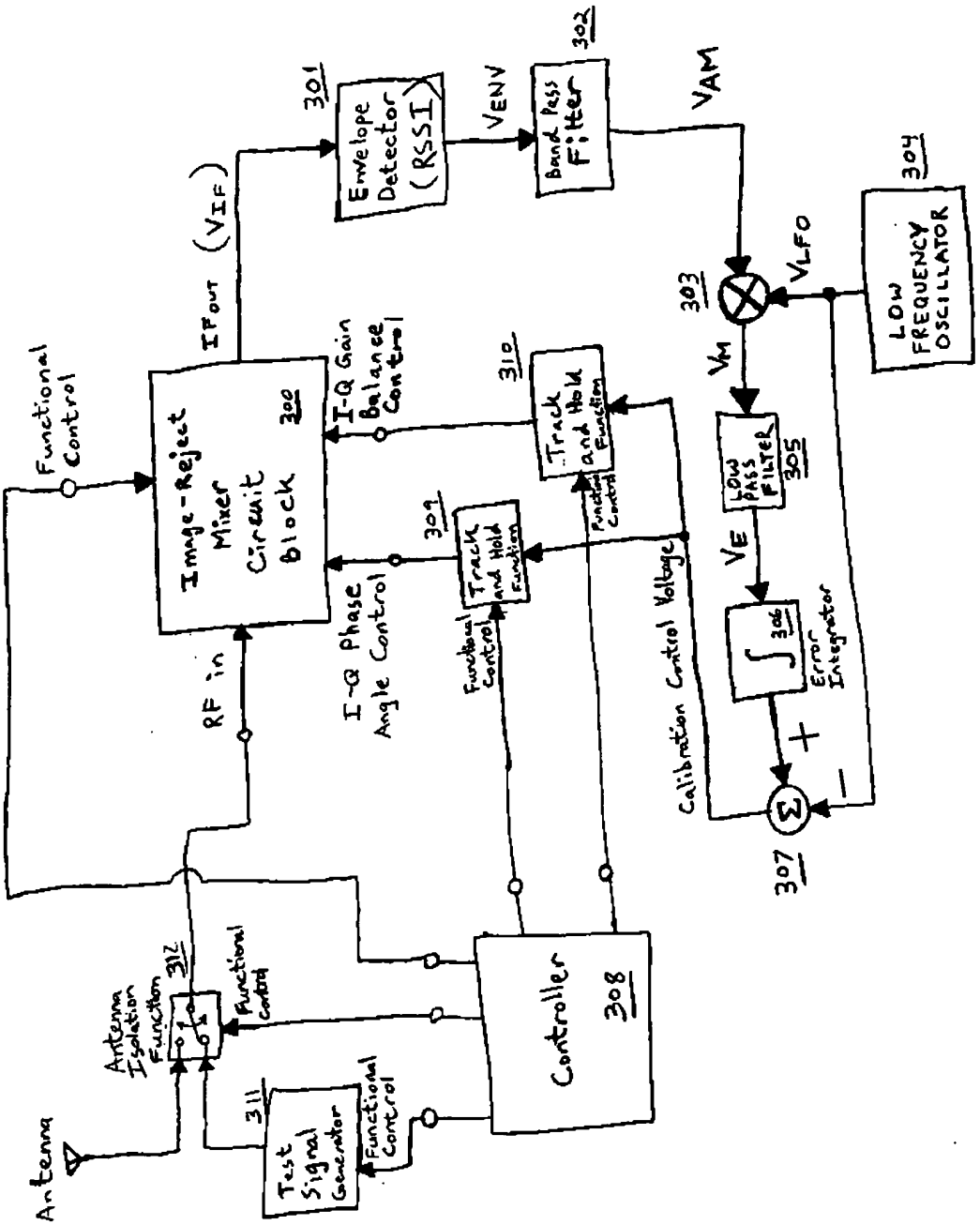


Figure 3.7 A Preferred Embodiment of an Image Reject Mixer Calibration Method Using Tau-Dither Tracking

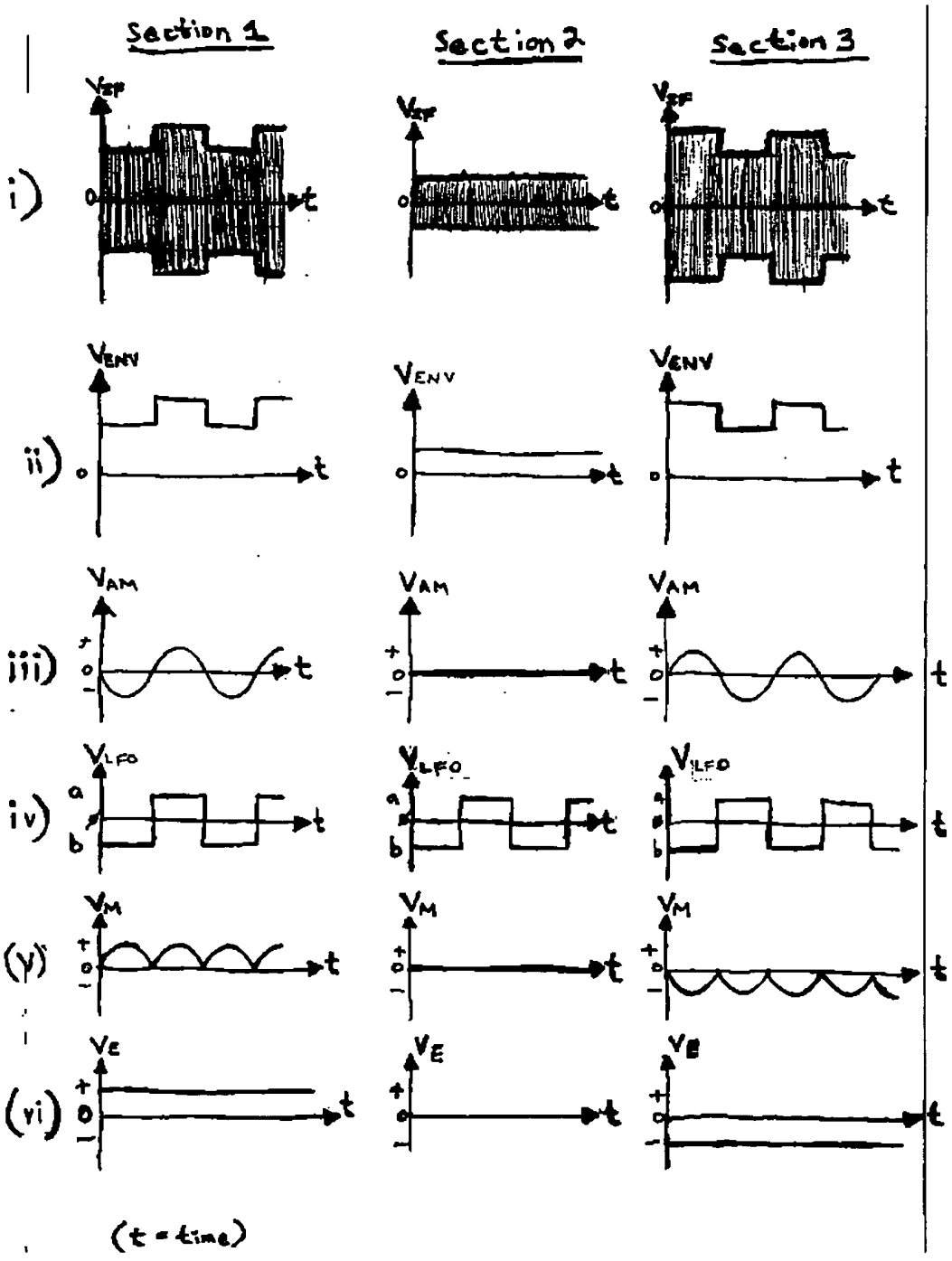


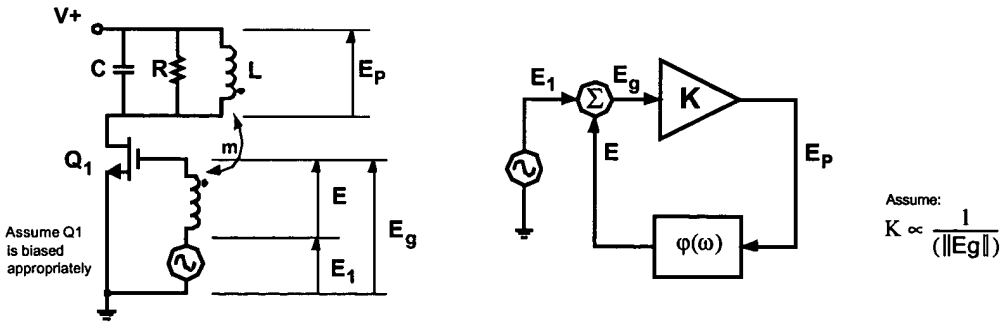
Figure 3.8 Waveforms Associated With the Tau-Dither based, Image-Reject Calibration Loop

Appendix A Adler's Theory of Injection Locking

The mathematical analysis of a non-linear injection locked oscillator can become extremely complicated. Many modern day microwave circuit simulators are evaluated by their ability to solve such systems. Fortunately, a very simple approach can be applied to the topology used in this thesis with sufficient accuracy to gain valuable insight into the operation and properties of an injection locked ring oscillator. The paper from which this theory is borrowed is famous for it's clarity of explanation and therefore much of the discussion below follows very closely to the style and presentation from that reference.

A.1 Classical Theory of Injection Locking

In 1946, Robert Adler presented a simplified theory for describing the injection locked behaviour of a triode oscillator[38]. A small portion of his theory will be described here with reference to a FET based oscillator having a similar topology:



a) Schematic b) Simplified block diagram

Figure A.1 Basic oscillator circuit

Voltages:

E_p = voltage across the tank
E = voltage induced in the gate coil
E_1 = voltage of injected signal
E_g = resultant gate voltage
Q = figure of merit of the tank L, C, R.

Angular Frequencies:

ω_o = free-running frequency
ω_1 = frequency of injected signal
$\Delta\omega_o = \omega_o - \omega_1$ = "undisturbed" beat frequency
ω = instantaneous frequency of oscillation
$\Delta\omega = \omega - \omega_1$ = instantaneous beat frequency

Figure A.1a shows a simplified FET oscillator circuit. The bias and characteristics of the device are not relevant towards this analysis and so the block diagram to the right is a valid representation. With no input signal present, the Barkhausen[39] criterion for oscillation will be satisfied at the frequency of ω_o. For our analysis, we will make the following assumptions to drastically simplify the analysis:

- Since this theory attempts to derive the rate of phase rotation from an instantaneous phase and amplitude knowledge, we implicitly assume that the system can have no "after effects" from different conditions which may have existed in the past.
- The frequency of the externally injected signal will be near the center of the pass band of the resonator within the condition of (A.1)

$$\frac{\omega_o}{2Q} \gg \Delta\omega_o \tag{A.1}$$

- Even though our system model is linear, we know that there must exist some limiting effect in the oscillator which will stabilize the amplitude of oscillation. We will assume that the time constant of the amplitude limiting mechanism is short compared to one beat cycle as stated in (A.2). This is usually true for oscillators which have "instantaneous" type limiting mechanisms.

$$T \ll \frac{1}{\Delta\omega_o} \tag{A.2}$$

- In addition we will further assume a weakly injected signal so that the AM variations of E will also be small compared to E itself, (.i.e. (A.3)).

$$E_1 \ll E \tag{A.3}$$

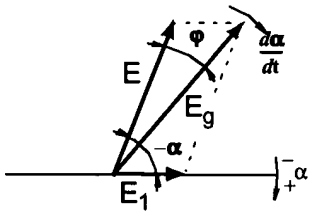


Figure A.2 Vector diagram of instantaneous voltages

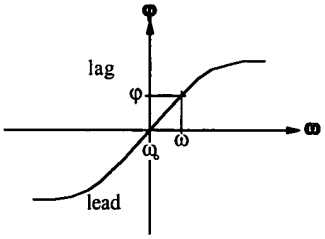


Figure A.3 Phase versus frequency for a simple tuned circuit

Let Figure A.2 be a vector representation of the voltages in the oscillator at a given instance. We will also let the injected signal E_I be stationary with respect to our eyes such that any other stationary vectors will also symbolize an angular frequency of ω_1. A vector which is rotating with an angular velocity of $\left(\frac{d\alpha}{dt}\right)$ represents an angular frequency of $\left(\frac{d\alpha}{dt}\right)+\omega_1$, or an angular beat frequency of

$$\Delta\omega = \frac{d\alpha}{dt}. \qquad (A.4)$$

The vector diagram therefore shows beat frequency and phase. It should be realized that $\left(\frac{d\alpha}{dt}\right)$ is an instantaneous angular frequency which can vary such that a complete beat cycle may never happen; the oscillator may become synchronized or locked first.

With no injected signal, $E_g = E$, and we know that the feedback circuit can only return E in phase with E_p at one frequency, the free-running frequency ω_o. Figure A.3 shows a typical

phase shift versus frequency curve for the single tuned circuit. With the input reference being the current through the tank and the output taken as the voltage across it (E_p). Amplitude limiting effects will typically cause the gain of the amplifying device to decrease as the oscillations grow. Eventually a stable amplitude level is reached where the gain of the device has decreased to unity.

Let an externally injected signal E_1 be introduced at frequency ω_1. Assume Figure A.2 shows an accurate representation of the voltage vectors at a given instance in the beat cycle. Feedback vector E lags behind E_g by a phase angle φ. This implies that the oscillator is no longer operating at it's free-running frequency and actually exceeds ω_0 by an amount which will result in a phase shift of φ in the tank.

From Figure A.2 we deduce

$$\varphi = \frac{E_1 \sin(-\alpha)}{E} = -\frac{E_1}{E}\sin\alpha . \tag{A.5}$$

We obtain the instantaneous frequency from the curve of Figure A.3, but with our assumption of (A.1), we can assume that we will be operating in the linear region of the φ versus ω curve with slope

$$A = \frac{d\varphi}{d\omega} . \tag{A.6}$$

Thus the phase angle for frequencies ω close to ω_0 will be

$$\varphi = A(\omega - \omega_o) . \tag{A.7}$$

Which can be expressed as

$$\varphi = A(\omega - \omega_o) = A[(\omega - \omega_1) - (\omega_o - \omega_1)] = A[\Delta\omega - \Delta\omega_o] . \tag{A.8}$$

Subbing (A.5) on the left and (A.4) on the right, we have

$$-\frac{E_1}{E}\sin\alpha = A\left[\frac{d\alpha}{dt} - \Delta\omega_o\right] . \tag{A.9}$$

With substitution

$$B = \frac{E_1}{E} \cdot \frac{1}{A} \tag{A.9a}$$

we get

$$\frac{d\alpha}{dt} = -B\sin\alpha + \Delta\omega_o \tag{A.9b}$$

Adding the injected frequency ω_1 to both sides we can also state

$$\omega = -B\sin\alpha + \omega_o \tag{A.9c}$$

This means that the oscillator's instantaneous frequency is shifted from the oscillator's free-running frequency by an amount proportional to the sine of the angle between the oscillator and the injected signal and all of the factors in B.

For a single tuned resonator, the phase shift can be expressed as

$$\tan\varphi = 2Q\frac{\omega - \omega_o}{\omega_o} \tag{A.10a}$$

which for small angles approximates to

$$\varphi = 2Q\frac{\omega - \omega_o}{\omega_o}. \tag{A.10b}$$

Substituting into (A.6) gives

$$A = \frac{2Q}{\omega_o} \tag{A.10c}$$

and

$$B = \frac{E_1}{E} \cdot \frac{\omega_o}{2Q}. \tag{A.10d}$$

Equation (A.9b) can then be rewritten for a single tuned circuit as

$$\frac{d\alpha}{dt} = -\frac{E_1}{E}\frac{\omega_o}{2Q}\sin\alpha + \Delta\omega_o \tag{A.11}$$

An injection locked, steady state is possible when the oscillator's phase is synchronized to that of the injection source such that their relative phases can be different, but not slipping with respect to one another; i.e. $\left(\frac{d\alpha}{dt}\right) = 0$ which means that all the vectors in Figure A.2 are stationary with respect to our reference E_1. In a locked state then,

$$0 = -\frac{E_1}{E}\frac{\omega_o}{2Q}\sin\alpha + \Delta\omega_o \tag{A.12a}$$

or

$$\sin\alpha = 2Q\frac{E}{E_1}\cdot\frac{\Delta\omega_o}{\omega_o}. \tag{A.12b}$$

(A.12b) describes the stationary phase angle between the injected signal and the oscillator. Since sin α can only assume values between +1 and -1, we can define the condition required for synchronization as

$$\left|2Q\frac{E}{E_1}\cdot\frac{\Delta\omega_o}{\omega_o}\right| < 1 \tag{A.13a}$$

or

$$\frac{E_1}{E} > 2Q\left|\frac{\Delta\omega_o}{\omega_o}\right|. \tag{A.13b}$$

For an oscillator without a single tuned resonator for a load, the criteria for synchronization can be described as

$$\frac{E_1}{E} > |A\Delta\omega_o| \tag{A.13c}$$

where $A = (d\phi/d\omega)$ for the particular type of load employed.

Equation (A.12b) can also be written more generally as

$$\sin\alpha = \frac{E}{E_1} A \Delta\omega_o \tag{A.14}$$

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